PRELIMINARY CONSOLE OPERATIONS GUIDE

INTRODUCTION

The console is made up of several functional units:

1. Console VDT/Printer
2. Input Keyboard
3. Console Switches
4. Function Switches and Indicators

Reference to IBM publication GA 26-5881, IBM 1130 Functional Characteristics, pages 114 to 123 of Revision 6, will explain the operation of the IBM 1130's console. The Console VDT/Printer, Input Keyboard, and Console Entry Switches function in a compatible manner except as noted. The Display Panel and Function Switches and Indicators offer enhanced control. See description of the individual units for further details.

Console VDT/Printer

The Console VDT/Printer is a program-to-operator output device. Program control is needed for the following two frequently performed operations:

1. Printing of output for program-to-operator communication.
2. Printing of input typed on the input keyboard for verification of operator initiated input.

All software which operates on the 1130's Console Printer will operate on the VDT or Printer except that some VDT's will not display a Line Feed. The VDT Display Area is narrower than the 120 position on the 1130's Console Printer. To allow 120 position of output on the VDT the hardware forces a Carrier Return, Indent, and the remaining columns are displayed. This action is transparent to the program. Only 2 tabs are supported and they are preset at columns 20 and 36. The Console Printer on the 2130 is compatible with the 1130's. Both the Console VDT and Console Printer may be located up to 10' from the CPU.

Input Keyboard

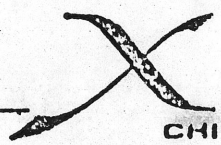
The Input Keyboard's primary function is to provide a means for operator-to-system imput. Operation of a character key on the Keyboard does not in itself cause printing at the Console VDT/Printer; the Keyboard and Console VDT/Printer combinations do not automatically function like a typewriter; each must be separately program-controlled. The NUM shift key must be held to enter the number shift characters into the program. The Keyboard is otherwise in Alpha mode.

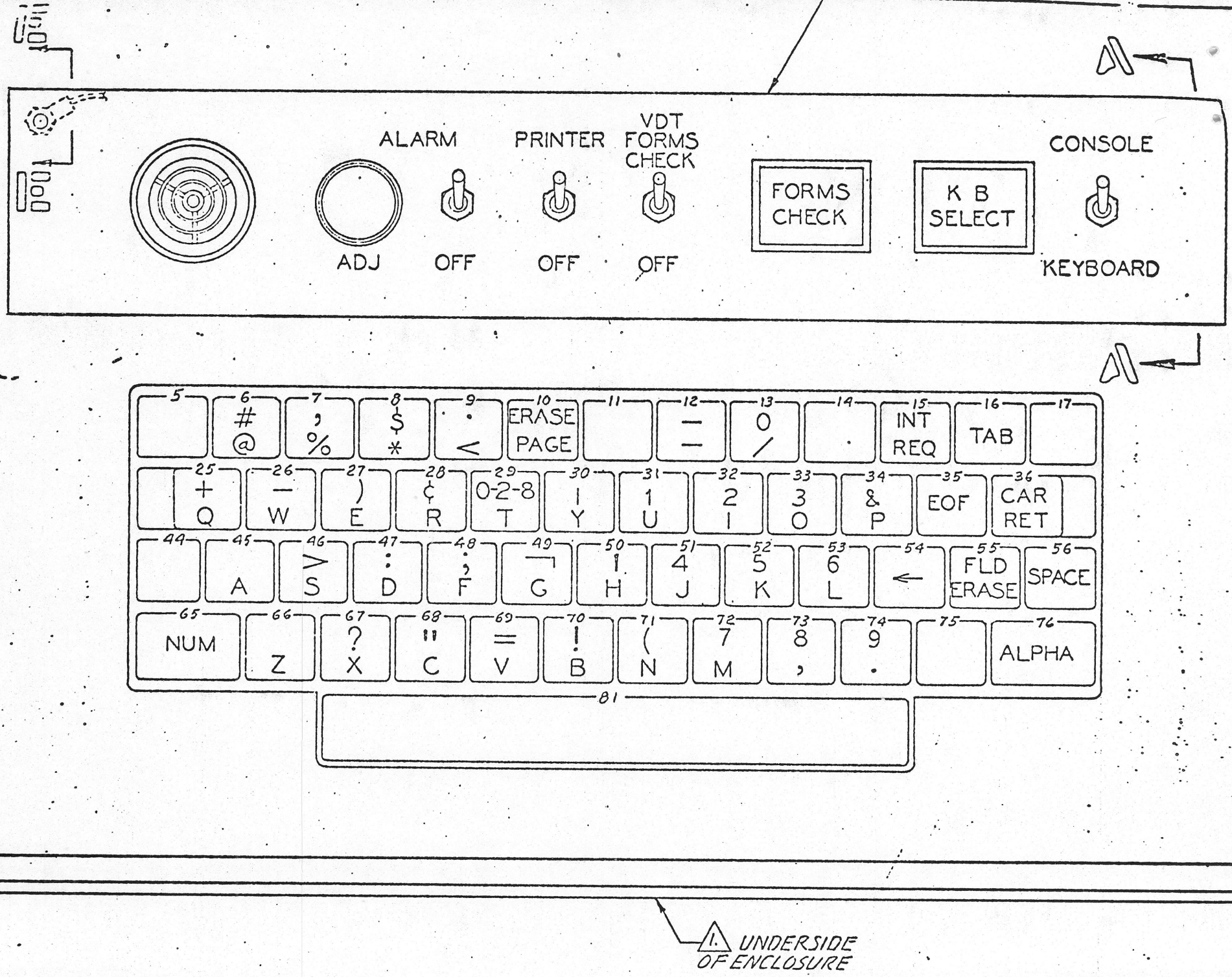
Additional Switches and Indicators on the Keyboard are, from left to right:

Alarm - Creates an audible indication of a Carrier Return if turned on.

Alarm Adjustment Switch - Adjusts duration of alarm.

Alarm On/Off Switch - Enables or disables the alarm.




ALARM
PRINTER
VDT FORMS CHECK
CONSOLE
ADJ
OFF
OFF
OFF
FORMS CHECK
K B SELECT
KEYBOARD
ERASE PAGE
INT REQ
TAB
EOF
CAR RET
FLD ERASE
SPACE
NUM
ALPHA
1. UNDERSIDE OF ENCLOSURE

Print On/Off Switch - Enables or disables parallel Printer which must be compatible to Console VDT with respect to baud rate, special control characters, etc.

VDT Forms Check Switch - If on, sends a paper low indicator to the CPU when the VDT screen is full. This allows the program to prevent the next line from being written to the VDT. If off, allows the VDT screen to roll upward one line as each additional line is output. This data rolled from the top of the screen is lost. Programs will soon be available to write this data to a disk file and dump it to the system printer.

VDT Forms Check Indicator - Is illuminated when the VDT Forms Check is on and the screen is full. The Erase Page Key may be pressed or the VDT Forms Check Switch must be turned off then Start pressed to proceed.

Keyboard Select Indicator - Is illuminated when the Keyboard is selected and operator action is expected.

Console/Keyboard Switch - Select either the Keyboard or the Console Entry Switches as the input source. Effect determined solely by the program.

Additional keys on the Keyboard are:

Erase Page - Erases the VDT and has no effect on the program, is used with the VDT Forms Check Switch.

Tab, Car Return and Space - Are replacements for the equivalent switches on the front of the 1130's Console Printer.

The Keyboard may be placed up to 10' from the CPU.

Console Entry Switches

Console Entry Switches are used only under program control to enter data. This can be done while the CPU is operating. Their function is compatible with the 1130's Console Entry Switches. Entering data into addressed storage by means of manual control is accomplished through the Data Entry Keyboard and Console Function Switches.

Function Switches and Indicators

These switches and indicators are located on the main processor panel.

INDICATORS

The Parity Indicator - Turns on when a parity error is detected in a word read out of main memory.

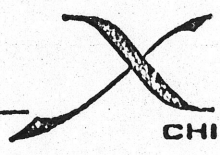
The S. P. Check Indicator - Turns on whenever a Storage Protect check is detected. This feature is not enabled in the 1130 replacement.

The OPR Check Indicator - Turns on when an invalid operation code is detected.

The Wait Indicator - Turns on when the CPU has detected a WAIT instruction.

The Run Indicator - Turns on when the CPU is operating.

The ACC/Data Display Indicators - Displays the contents of the accumulator in Hex when the Mode Control Switch is not in Console, IAR or SAR Compare.



When the Mode Control Switch is placed in the Console mode, the display reflects the contents of the Hex Key Data Register. If the contents of the addressed storage is displayed by operating the Display button the ACC/Data Display will show the contents of the SBR (Storage Buffer Register) in Hex. If new data is entered through the Data Entry Keyboard, the display will revert to the contents of KDR (Hex Key Data Register). In IAR Comp mode or SAR Comp mode, the ACC/Data displays the address to be halted and then blinks when that address is reached.

The Instruction Address Indicator - Represents the status of the 16 bits in the instruction address register. The instruction address register holds the address of the next sequential instruction.

The Storage Address Indicator - Represents the status of the 16 bits in the storage address register.

The storage address register contains the address of the last reference to addressed storage.

The Storage Buffer Indicator - Represents the status of the 16 bits in the storage buffer register.

The storage buffer register is the buffer for addressed storage. Each word of data transferred into addressed storage passes through the storage buffer register.

The Accumulator Indicator - Represents the status of the 16 bits in the accumulator register.

Data can be loaded into the accumulator register from

addressed storage; conversely, data can be stored in addressed memory from the accumulator register. Data in the register can also be shifted to the right or to the left and can be manipulated by arithmetic and logical instructions. The accumulator register contains the binary number or expression resulting from an arithmetic or logical operation.

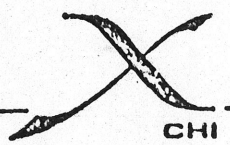
Error conditions, which are generally not-ready conditions or FORTRAN pause conditions, are indicated by the accumulator indicator. The ACC/DATA DISPLAY reflects in the Hex the contents of the accumulator when the Mode Control Switch is in Run, SI, SMC, or SS mode.

The Data Register Indicator - Represents the contents of the Data Register selected by the Register Select Rotary Switch.

The Condition Indicator - Represents the status of the Carry Indicator (C); the Overflow Indicator (OV); the Parity (P) bit, on when bits 0-15 of the SBR contain an even number of bits, and the Storage Protect (SP) bit, on when a word has been storage protected.

The Integrated File Adaptor (IFA) Select Indicators - Reflect the status of which of the five discs is selected by the IFA.

The Operation Register Indicator - Indicates the contents of all sixteen bits of the last instruction accessed by the processor. The indicator display is partitioned and labeled so that the OP code, displacement, Format, Tag and other special purpose bits can be identified.



The Machine Cycle Indicator - Reflects the type of machine cycle in process. The Indicators I1, I2, and IA are compatible to their equivalents on the 1130. The II indicates a double indirect cycle, the E and the E1 together indicates an E1 cycle, the E alone indicates any other E cycle, ie. E2 or E3. The F Indicator is not used at this time. The X7 Indicator turns off when a cycle steal is in process.

The Interrupt Level Indicator - Shows the interrupt level(s) active or pending.

The following devices interrupt on the levels shown:

A - Internal

B - Internal

0 - 1442 Card Device

1 - Synchronous Communications Adaptor

2* - Disc Drive

3* - 1627 Plotter

- 718 Plotter

- 2250 Display Unit

- System 7

- Interval Timer**

- Comm Line**

4* - 2155 Paper Tape Punch**

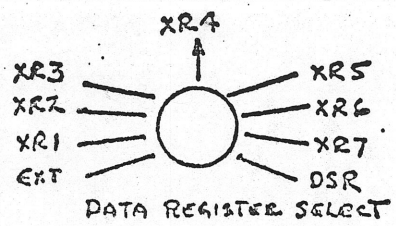
- 2134 Paper Tape Reader**

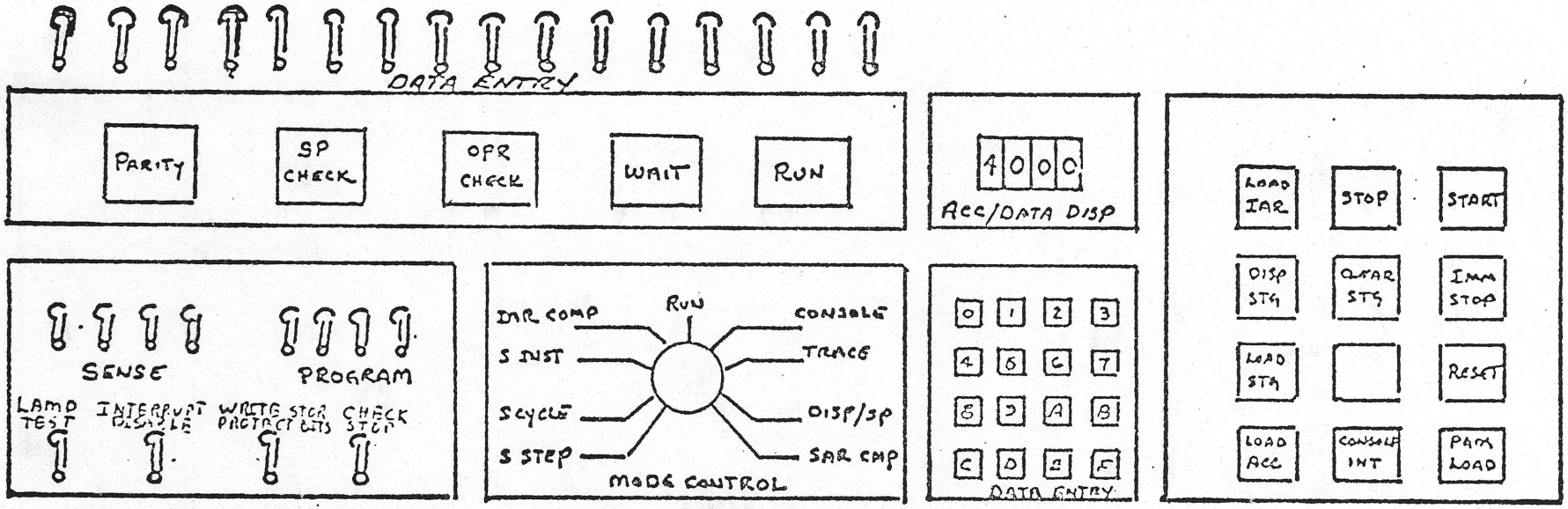
- 1103 Line Printer

- 1442 Card Device

- 2101 Card Reader

- Console Interrupt/Interrupt Request Key


XR4
XR3
XR2
XR1
EXT
XR5
XR6
XR7
DSR
DATA REGISTER SELECT


DATA ENTRY
PARITY
SP CHECK
OPR CHECK
WAIT
RUN
4000
ACC/DATA DISP
LOAD IAR
STOP
START
DISP STG
QUAR STG
IMM STOP
LOAD STG
RESET
LOAD ACC
CONSOLE INT
PAM LOAD
SENSE
PROGRAM
LAMP TEST
INTERRUPT DISABLE
WRITE PROTECT
STOR BITS
CHECK STOP
DAR COMP
RUN
CONSOLE
S INST
TRACE
S CYCLE
DISP/SP
S STEP
SAR CMP
MODE CONTROL
0 1 2 3
4 5 6 7
8 9 A B
C D E F
DATA ENTRY

5* - Program Stop Key

* May be SAC Device

** May be configured to other interrupt levels

The CYCLE Control Count Indicator - Represents the value contained in the shift counter.

SWITCHES

The following switches on the CPU front panel control the displays and the operation of the CPU.

The Data Register Select Switch - Selects the register to be displayed in the Data Register Indicator. Registers which may be selected are:

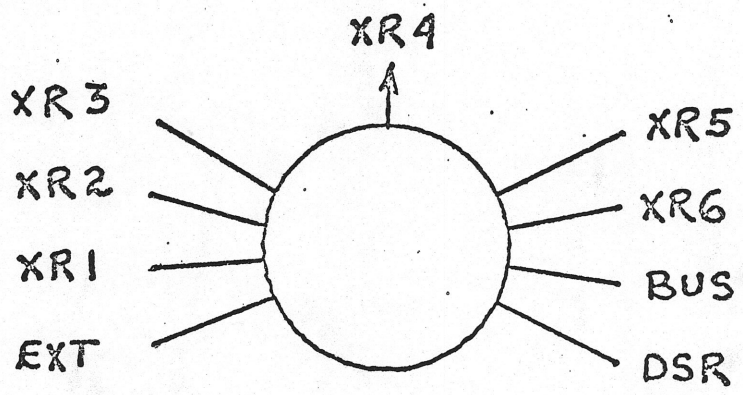
EXT - The Accumulator Extension Register. This register and the accumulator register are used as a 32 bit register. The 16 bit accumulator extension register is the low-order extension of the accumulator register. The accumulator extension register receives the data shifted to the right by the accumulator register or by a load double command code. The accumulator extension register is also used for multiplication and division operations and double-word arithmetic.

XR1 through XR6 - Index Registers 1 through 6 respectively.

BUS - Indicates the data on the internal bus of processor. (Primarily a CE Indicator)

DSR - Not implemented at this time.

The Sense and Program Switches are not used in 1130 mode.



DATA REGISTER SELECT

The Lamp Test Switch - Turns on all the indicators on the front panel. Defective bulbs can be found with this switch. This switch has no effect on the CPU operations.

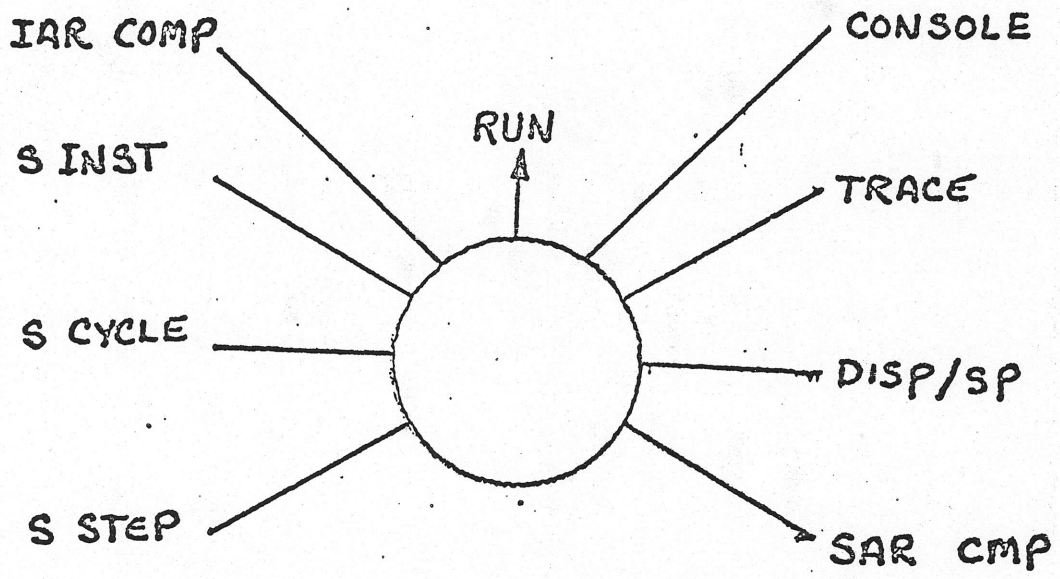
The Interrupt Disable Switch - Prohibits interrupts, levels A, B and 0-4, from affecting the machine. It should be used for hardware debugging only.

The Write StoreProtect Bits Switch - Allows addressed storage to be storage protected on a word basis. This switch is not used in 1130 mode.

The Check Stop Switch - Stops the machine at the end of the machine cycle in which a Parity Check or an OPR Check has occured. This switch should be left on for normal 2130 operation.

The Mode Control Switch - The Mode Control Switch selects one of the nine operating modes:

1. S Step (Single Step) Setting with each depression and release of the start key, causes the 2131 clock to advance one step; example, from T1 to T2. Switching to SMC mode completes the current cycle.
2. SMC (Single Machine Cycle) Setting with each depression of the start key, causes the central processing unit to advance one machine cycle; for example I1 to I2.
3. SI (Single Instruction) Setting causes the 2131 to interpret and execute a single instruction when the start key is pressed.
4. The IAR CMP (Instruction Address Register Compare) Setting stops the CPU at T7 of the I1 cycle.



MODE CONTROL

when the Instruction Address Register compares exactly with the value entered in the ACC/Data Display. The sequence of operations is:

1. Turn Mode Control Switch to Console
2. Enter STOP address through Data Entry Keyboard in Hex
3. Turn Mode Control Switch to IAR CMP
4. Press Start

When the desired address is reached, the CPU will stop and the ACC/Data Display will blink on and off. Pressing Start will continue execution in SMC mode until the instruction is completed.

5. The Run Setting causes the 2131 to advance through its stored program when the start key is pressed, or an interrupt occurs.

6. The Console Setting causes the data entered through the Data Entry Keyboard to be shifted through the ACC/Data Display. Use of the Load IAR, Load STG, and Load ACC Switches will cause the value in the ACC/Data Display to be loaded into addressed storage or register named.

To use the Console Setting when the machine is in the run state, press the Program Stop Key, IMM Stop Key, or turn the Mode Control Switch to Console. Pressing Program Stop causes a level 5 interrupt and should be done only if program is provided. Pressing IMM Stop may cause data loss and the instruction may not be complete as the

last cycle may not be finished. Check the Operation Register to insure that the appropriate indicator is illuminated on the Machine Cycle Indicator. Turning to Console mode causes the machine to go into Single Instruction (SI) mode. This should complete the cycles required. Should an interrupt be pending, the forced BSI will take place the next time Start, LD IAR, or LD STG is pushed. This may not be desirable. To remedy this situation, put the Mode Control Switch in SI mode, noting the IAR, then service the interrupt, load the IAR with the previous value and proceed.

7. The TRACE Setting causes a level 5 interrupt after each mainline program instruction is completed, except XIO, BSI, and BOSC.

8. The DISP/SP Setting displays addressed storage consecutively when Start is pressed (the Storage Protect feature is not implemented at this time).

9. The SAR CMP Setting stops the CPU at T7 with the ACC/Data DISP blinking when the address previously entered through the Data Entry Keyboard is referenced during program execution. This sequence is similar to IAR CMP except that the Mode Control Switch is turned to SAR CMP and Start is pressed. See IAR CMP above.

The Data Entry Keyboard - Only used when the Console Mode Switch is in Console mode. Hex digits are entered and are shifted from right to left through the ACC/Data Display.

If more than four digits are entered, only the last four remain. When the proper value is in the ACC/Data Display pressing one of the Function Switches, Load IAR, Load STG, and Load ACC, will use this value for the indicated function. See the description of the specific switches for detailed instructions. This value may also be used with the Mode Control Switch to determine the stop address in IAR CMP or SAR CMP mode.

The Data Entry Keyboard has no effect unless the Console Mode Switch is in the console setting.

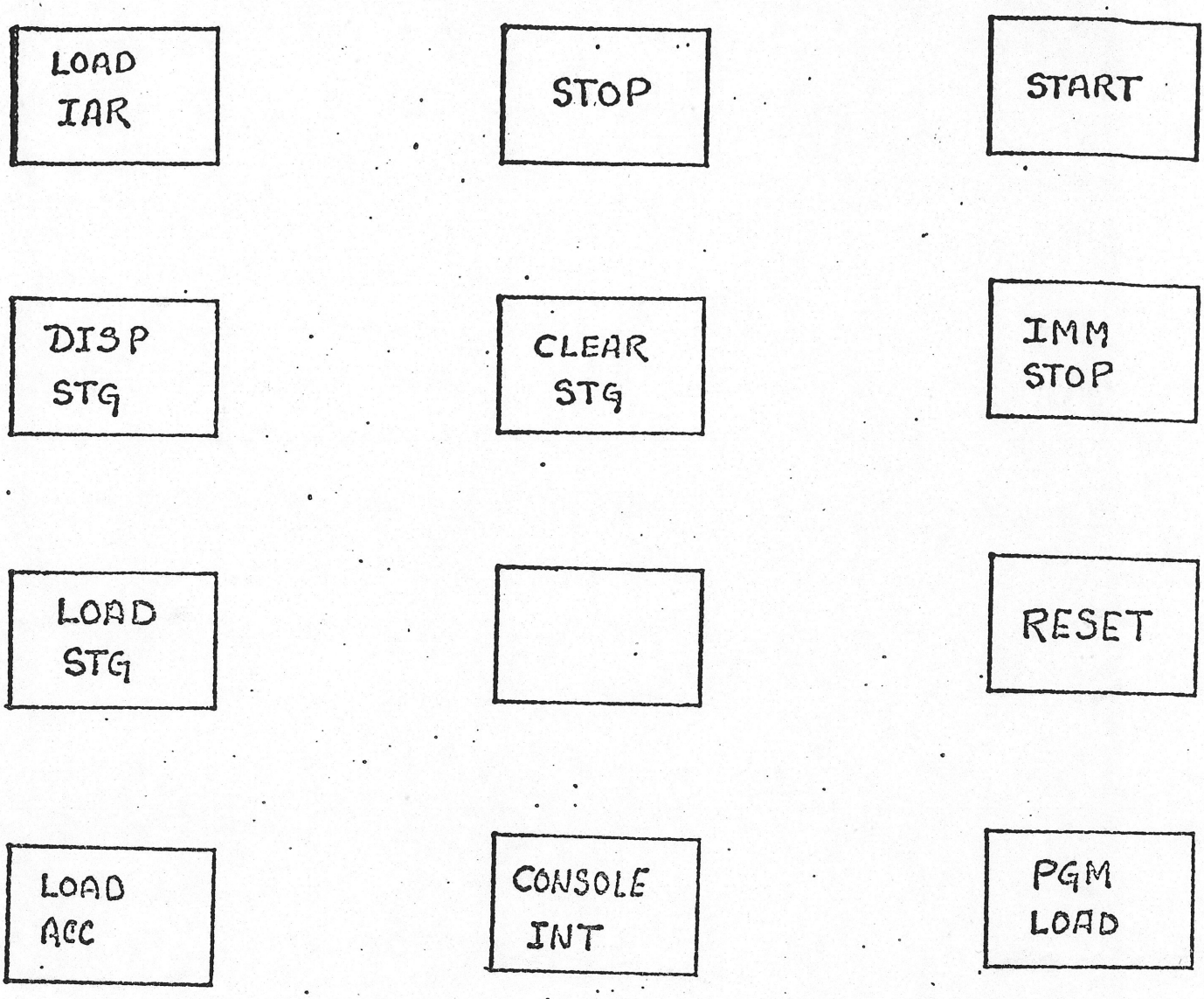
Function Switches

The LOAD IAR Switch (Load Instruction Address Register) - Causes value in the Hex Key Data Register (KDR) to be stored in the instruction address register. This switch operates only when the Console Mode Switch is in the Console setting.

The DISP STG (Display Storage) Switch - Causes the Instruction Address Register (IAR) to be transferred to the Storage Address Register (SAR) and displays, in the Storage Buffer Register (SBR), the contents of that main memory location. The IAR is then incremented by 1. This switch operates only when the Console Mode Switch is in the Console Setting.

The LOAD STG (Load Storage) Switch - Causes the Instruction Address Register (IAR) to be transferred to the Storage Address Register (SAR) and loads the value currently in the KDR Buffer into that location. This also is seen in the Storage Buffer Register (SBR). The IAR is then incremented by 1.

FUNCTION SWITCHES



This switch operates only when the Console Mode Switch is in the Console setting.

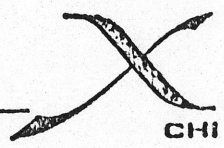
The LOAD ACC (Load Accumulator) Switch - Loads the value currently in the KDR into the Accumulator. This switch operates only when the Console Mode Switch is in the Console Setting.

The STOP Switch - Causes a level 5 interrupt. The program must then provide the control to cycle down I/O devices and stop the CPU. If routines that service this interrupt are not in the program, loss of information may result if the Program Stop Switch is operated.

The Clear STG (Clear Storage) Switch - Causes the status of the 16 Data Entry Switches to be loaded into each main memory location. This is the only way to load the values from the "bit" switches into main memory. The Start Switch must be pressed simultaneously with the Clear STG Switch and the Start Switch released first for successful operation. This loading will continue until IMM (Immediate Stop) is pressed or the Mode Control Switch is taken out of Run position.

The Console INT (Console Interrupt) Switch - Provides a second INT REQ (Interrupt Request) Switch for the 2130. There is no difference between INT REQ on the Keyboard and Console INT on the Console.

The Start Switch - Causes the 2131 to take one clock step or one machine cycle (and to continue taking additional



cycles) depending on the setting of the Console Mode Switch and program. Eight clock steps complete one machine cycle, except some arithmetic operations, and one or more machine cycles complete an instruction.

The IMM (Immediate) Stop Switch - Causes an immediate stop of the processor interrupt, although the input/output devices will finish their present cycle. Data from the devices may be lost if they are operating when the IMM Stop key is pressed. A complete program restart is normally required.

The Reset Switch - This switch operates only when the CPU is not running. This resets all input/output and machine register, cycle and control triggers, and status indicators.

The PGM Load (Program Load) Switch - Causes the IPL device to execute its program load cycle and load, addressed storage, beginning at location 0000. There must be no other Function Switch pressed after Reset if PGM Load is to be operated. Mode must be Run, SI, or SMC.

Notes on Using the 2130 Console

To Abort a Job Under DM2:

1. Press INT REQ on keyboard or press Console INT on the console. This will usually cause a flush to the next card.

To Change the IAR (Manual Branching):

1. Turn the Mode Control Switch to Console.
2. Enter the desired address in the Data Entry Keyboard, high order hex digit firts.
3. Press Load IAR.
4. Turn the Mode Control Switch to Run.
5. Press Start to resume execution.

To Display a Addressed Storage Location:

1. Turn the Mode Control to Console.
2. Enter the Storage location in the Data Entry Keyboard, high order hex digit first.
3. Press Load IAR.
4. Press DISP STG.

At this time another address may be entered, a value may be loaded into addressed storage, or the Mode Control Switch may be set to Run and the Start Switch pressed to resume execution if next address is a valid instruction.

To Modify a Addressed Storage Location:

1. Turn the Mode Control to Console.
2. Enter the Storage Location in the Data Entry Keyboard, high order hex digit first.
3. Press Load IAR.
4. Enter the desired value in the Data Entry Keyboard, high order hex digit first.

5. Press Load STG.

To Load the Accumulator:

1. Turn the Mode Control Switch to Console.
2. Enter the desired value in the Data Entry Keyboard, high order hex digit first.
3. Press Load ACC.

ISS SUBROUTINE WAITS

ACCUMULATOR Display	Device Causing Wait	Cause of Wait
/1000	Card Read/Punch	Device is not ready, or last card indicator is on or read.
/1001	Card Punch	Illegal device, device is not in system, illegal function, word count is over +80, or word count is zero or negative.
/100F		This wait occurs in a DUP operation after a D112 error message has been printed.
/2000	Keyboard/Console Printer/Teletypes	Device is not ready.
/200X		Keyboard input is expected from typewriter X.
/4000	Card Reader	Device is not ready.
/4001		Illegal function, word count is over +80, or word count is zero or negative.
/9000	Printer	Device is not ready or end of forms. Make device ready and press PROGRAM START.
/9001		Illegal function, word count is over +60, zero or negative. To retry operation, press PROGRAM START (PRNT3 only).
/9002		Parity check, scan check, or ring check. Reset check and press PROGRAM START. The operation is not retried (PRNZ only).

INSTRUCTIONS ADDED TO THE 2130

The register to register and register to memory are added instructions not availible on the 1130. Three work registers have also been added to the 2130 to increase computing capability.

OP code for all register operations: 01011

DEFINITIONS:

Registers; index registers 1,2,3; workregisters 4,5,6; IAR 0; ACC A
These characters represent the appropriate register.

X register - specified in the "tag" column (32) also the result register

Y register - specified in the "operand" column (35-72)

INCREMENT REGISTER STATEMENT (RINC)

The RINC statement is used to increment the value of the specified X register by 1. It is valid in short format only.

Label (21–25)	Operation (27–30)	F (32)	T (33)	Operands & Remarks (35–55)
label	RINC		X	INCR REG X BY 1

DECREMENT REGISTER STATEMENT (RDEC)

Same as "RINC" but the register is decremented by 1.

Label (21–25)	Operation (27–30)	F (32)	T (33)	Operands & Remarks (35–55)
label	RDEC		X	DECR REG X BY 1

ADD REGISTER TO REGISTER, ADD MEMORY TO REGISTER (RADD)

The "RADD" statement in short format will add the X register to the Y register leaving the sum in the X register.

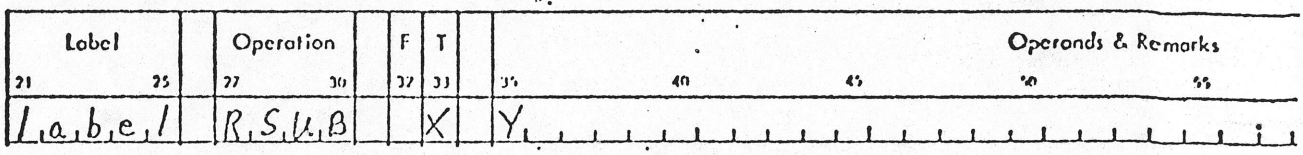
The "RADD" statement in long format will add the value specified in the operand to the value in the X register leaving the result in the X register.

The "RADD" statement in the indirect format will add the contents of the location specified in the operand field to the X register leaving the result in the X register.

Label (21–25)	Operation (27–30)	F (32)	T (33)	Operands & Remarks (35–55)
label	RADD		X	Y
label	RADD	L	X	ABSOLUTE VALUE
label	RADD	I	X	operand

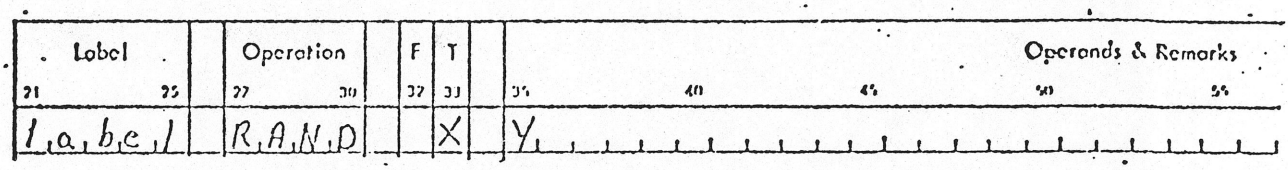
SUBTRACT REGISTER TO REGISTER, SUBTRACT MEMORY FROM REGISTER (RSUB)

The "RSUB" instruction is handled like the "RADD" except subtraction will take place instead of addition.



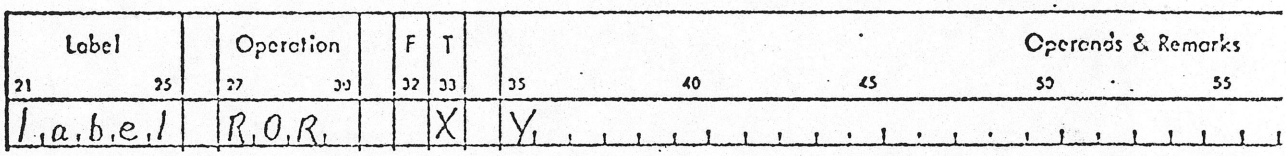
AND REGISTER TO REGISTER, AND MEMORY TO REGISTER (RAND)

The "RAND" instruction is handled like the "RADD" except 'AND'ing takes place.



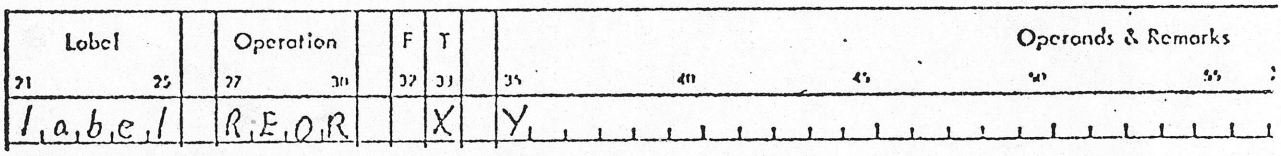
OR REGISTER TO REGISTER, OR MEMORY TO REGISTER (ROR)

The "ROR" is handled like the "RADD" except 'OR'ing takes place.



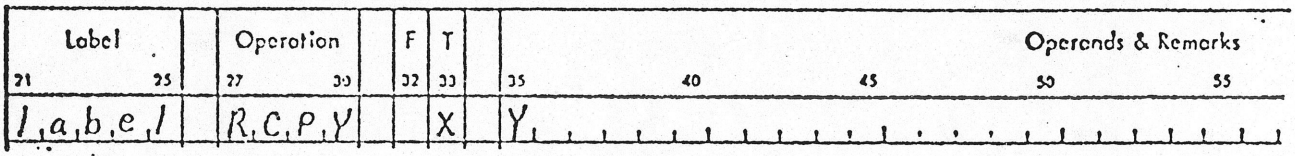
EOR REGISTER TO REGISTER, EOR MEMORY TO REGISTER (REOR)

The "REOR" ishamdled like the "RADD" except 'EOR'ing takes place.



COPY REGISTER TO REGISTER (RCPY)

The "RCPY" instruction replaces the value in the X register with the value of the Y register. This instruction valid in short format only.



LOAD REGISTER FROM MEMORY (RLD)

Loads the X register with the value in the operand in long format.
Loads the X register with the value specified by the address in the operand in the indirect format.

Label	Operation	F	T	Operands & Remarks
21 25	27 30	32	33	35 40 45 50 55
Label	RLD	L	X	ABSOLUTE VALUE
Label	RLD	I	X	operand

DOUBLE INDIRECT ADDRESSING

The letter 'D' in the format field of an instruction specifies double indirect effective address calculation.

Effective addr = c(c(addr))

DOUBLE INDIRECT addressing is not usable with these instructions:

1. all branch instructions
2. register operations (RR ops)
3. modify memory instructions

DEFINE CONSTANT BINARY

DCB (single word)
DCBD (double word)

Defines a constant as a 'DC' or 'DEC' but the value is specified in binary (1's and 0's).

ASCI (define a literal constant in ASCII code)

Same as the 'EBC' statement except ASCII is generated instead of EBCDIC. Parity can be specified in the format location. (col 32)

COLUMN 32

blank or 0 - bits 0 and 8 = 0
1 - bits 0 and 8 = 1
2 - bits 0 and 8 = even parity
3 - bits 0 and 8 = odd parity

Label	Operation	F	T	Operands & Remarks
21 25	27 30	32	33	35 40 45 50 55
Label	DCB			1010101010 — ETC 16 BITS
Label	DCBD			1010101010 — ETC 32 BITS
Label	ASCI	P		COMMENT

2130 Interrupt Control Instructions

This feature is accessed via an XIO instruction, with an IOCC for Area Code 7, function control (3Cxx). The following options are selected by bits 8 and 9 of the 2nd word of the IOCC:

1. Bit 8 on - Mask/Unmask interrupt levels as indicated by bit settings described below.

2. Bit 8 off - Cause Programmed Interrupt on interrupt levels as as indicated by bit settings described below.

3. Relocate Interrupt Transfer Vector - Bit 9 on - moves the ITV to locations /8006-/800D. This function is performed only once, and can be reset only by Master Reset. IOCC MUST HAVE BOTH 8 & 9 ON

The interrupt level selections are accomplished by turning on the IOCC bits as indicated in the following table:

Level	Bit	IOCC word	ITV Location
A	0	1	/0006 or /8006
B	1	1	/0007 or /8007
0	10	2	/0008 or /8008
1	11	2	/0009 or /8009
2	12	2	/000A or /800A
3	13	2	/000B or /800B
4	14	2	/000C or /800C
5	15	2	/000D or /800D

Enable/Disable High Core

This feature allows program control of High Core enable/disable. The instruction is LDX Long-format, with bit 10 on. Bit 11 then determines whether the function is enable (bit 11 = 1) or disable (bit 11 = 0). The Tag field must be 00.

Examples:

Disable Aux core -

```
DC      /6420
DC      *
```

Enable Aux core -

```
DC      /6430
DC      *
```

Disable Aux core and Branch Indirect through Addr -

```
DC      /64A0
DC      ADDR
```

Enable Aux Core and Branch to Addr -

```
DC      /6430
DC      ADDR
```

If the ITV has been relocated as described above, then all interrupts automatically enable aux core. This is, however, independent of the condition set by the special LDX, which will again become effective upon exiting the interrupt level.