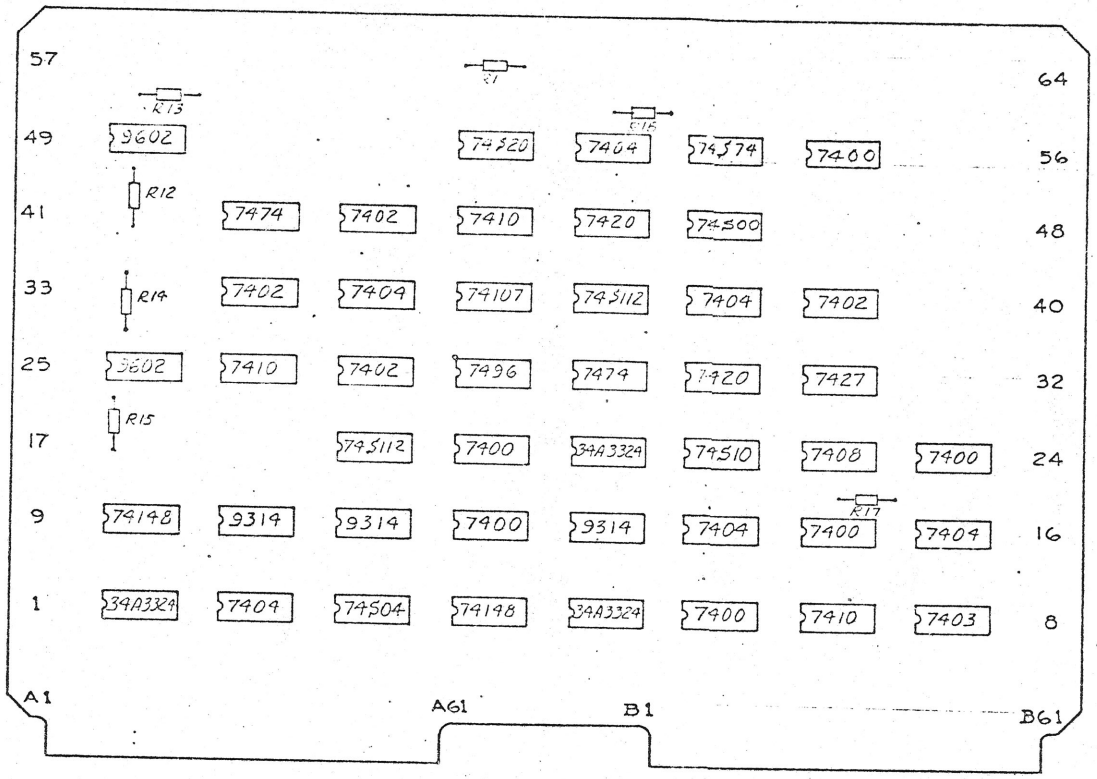
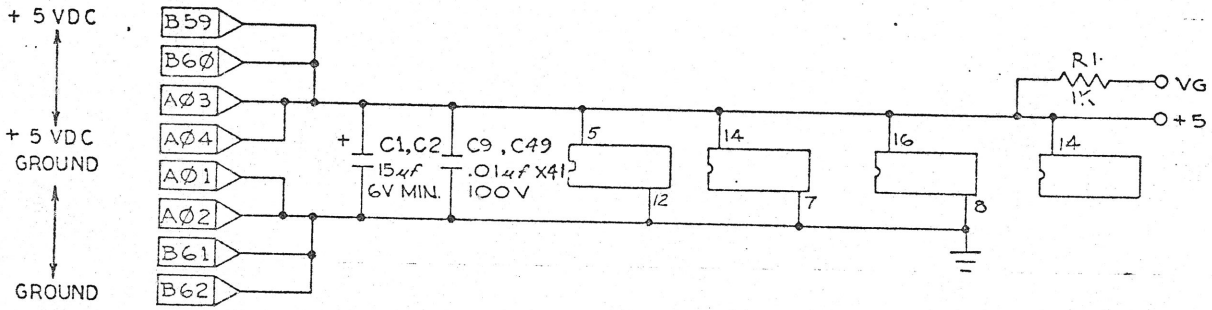
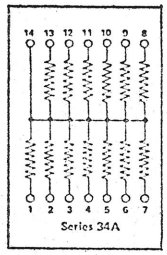
NOTES:
1- DELETED.

ASSEMBLY REVISION DATA (REF)		
REV. LTR.	DESCRIPTION	REASON







CONFIGURATION TABLE		
SC-2154	PC-2155	AC-2156
REV J	REV A	REV K

CONFIGURATION TABLE					
SCHEMATIC	REV	PC	REV	ASSY	REV
SC-2154	NC	PC-2155	NC	AC-2156	NC
SC-2159	NC		NC		A
	A		NC		B
	B		NC		C
	C		NC		D
	D		NC		E
	E		NC		F
	F		NC		G
	G		A		H
	H		A		J

LAST USED TABLE	
CODE	REF DES
AE	R19
	D1
	C61

FILE NUMBER

QTY REQD	PART OR FILE NUMBER	NOMENCLATURE	MFG PART NO OR MATERIAL	MFG NAME OR SPECIFICATION	ITEM NO
		LIST OF MATERIALS			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGULAR ±°
DECIMAL 2 PLACE ± .020
DECIMAL 3 PLACE ± .010
BREAK SHARP EDGES MAX
ON ALL CORNERS MAX
ALL MACHINE SURFACES

LETTER	DATE	LTR	DATE
K		M	
CHANGE NO.	2154		

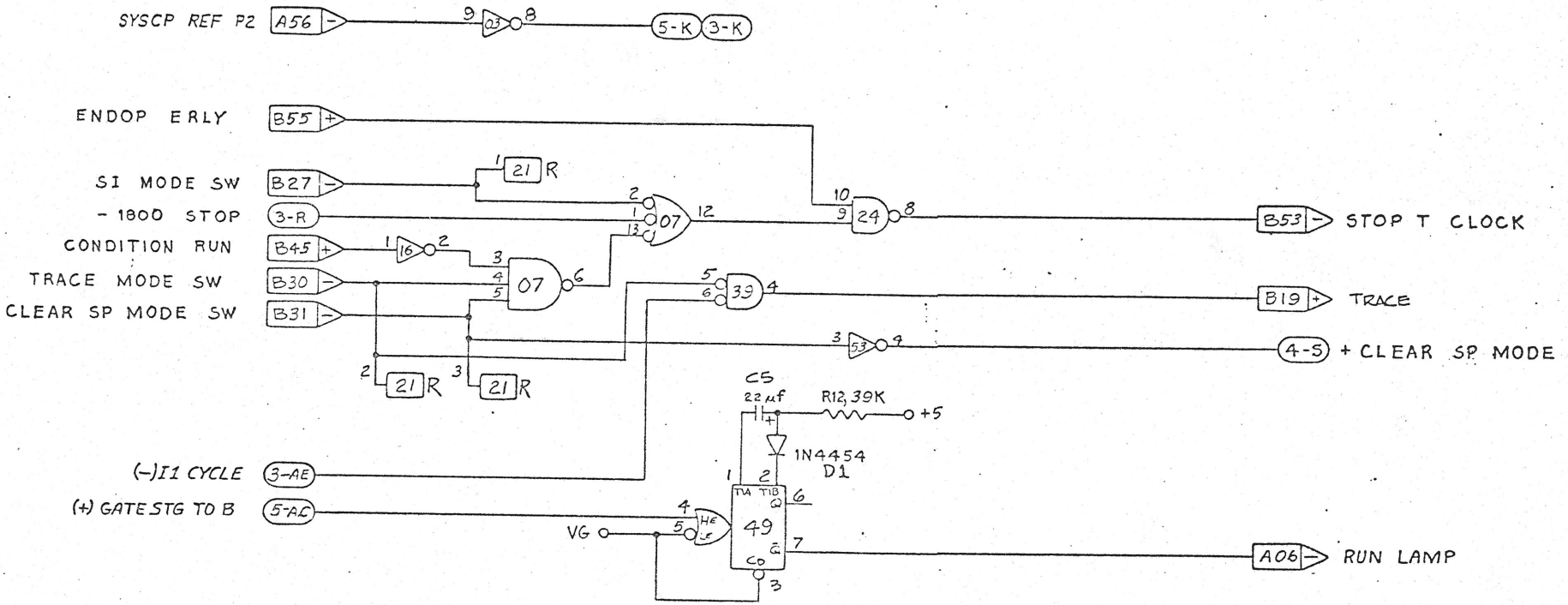
TITLE: CONTROL, FRONT PANEL-2131

COMPUTER HARDWARE, INC

DRAWN	AE 8/5/74	CHECKED	
DESIGN	TW		
DATE			

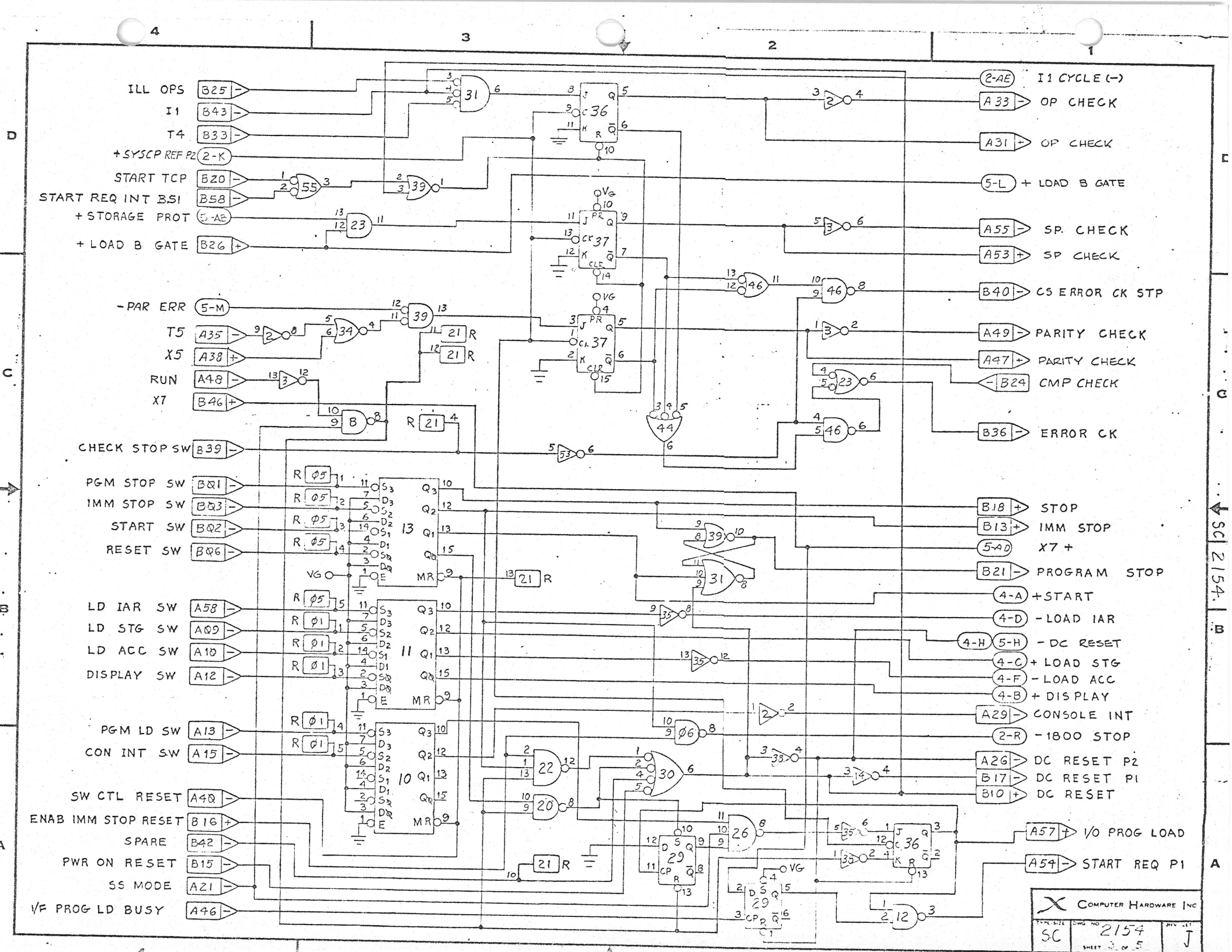
SC 2154 SHEET 1 OF 5

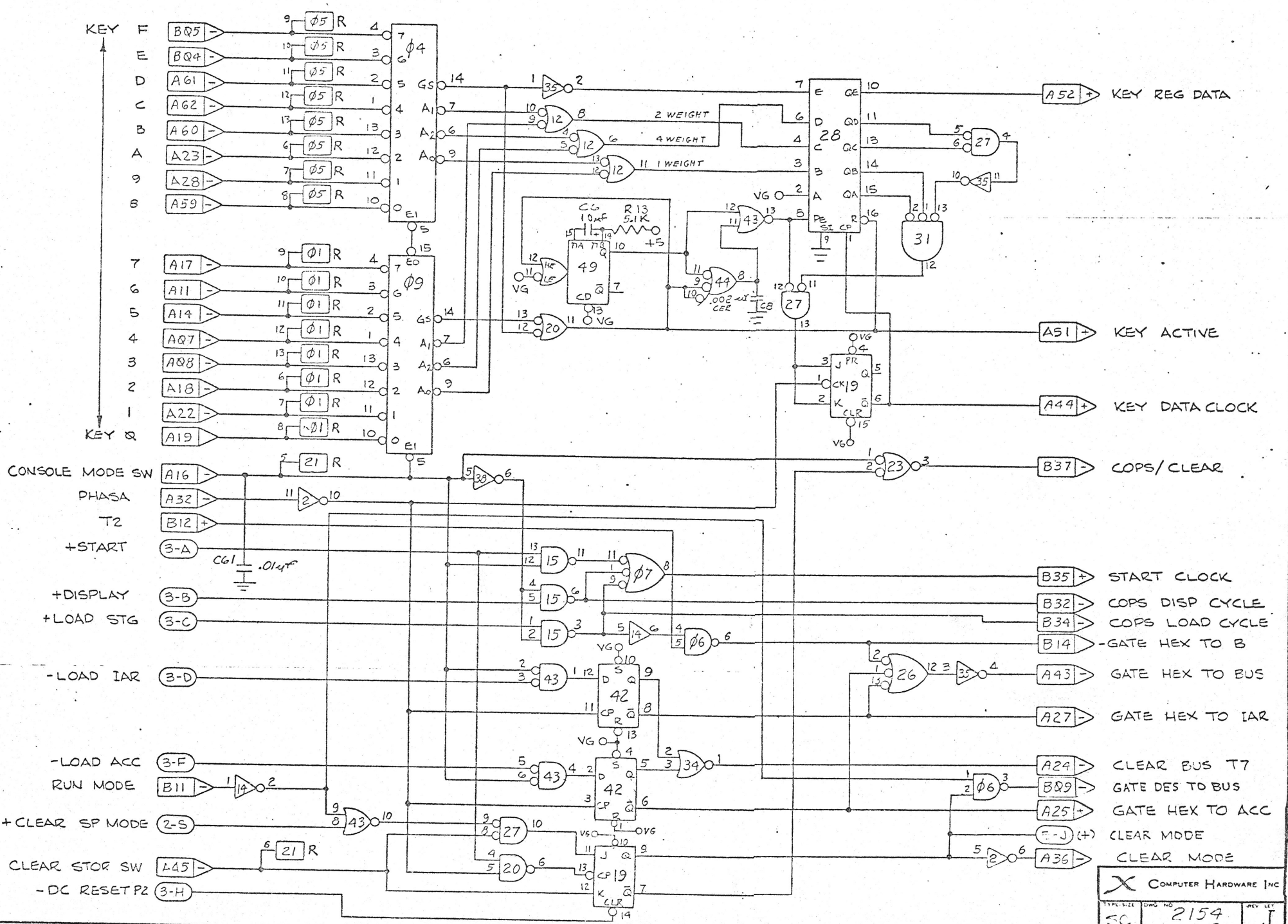
SIZE A — DWG NO 2096 — REV K

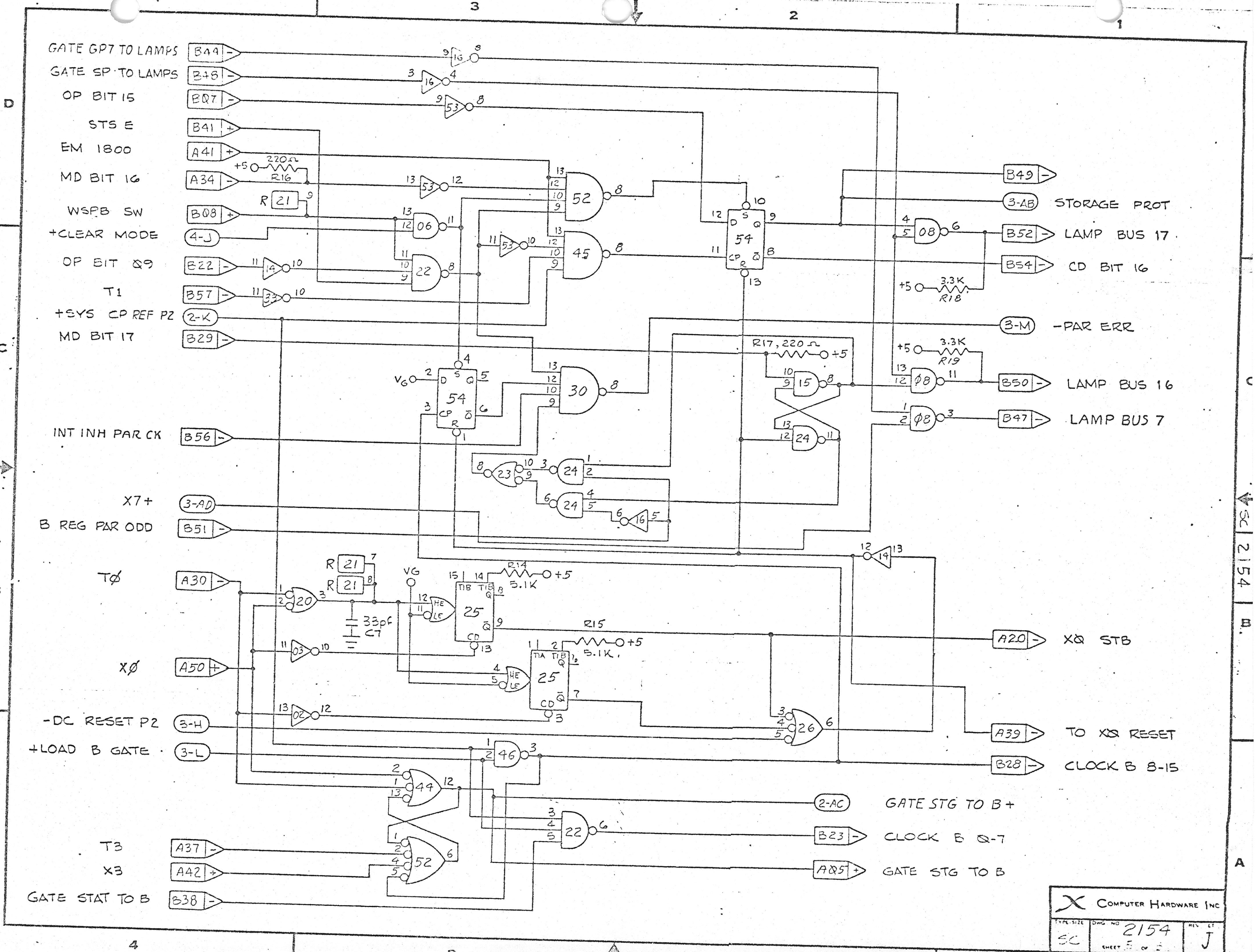


COMPUTER HARDWARE INC

TYPE-SIZE	DWG NO	REV LET
SC	2154 SHEET 2 OF 5	J


ILL OPS B25
I1 B43
T4 B33
+SYSCP REF P2 2-K
START TCP B20
START REQ INT BSI B58
+STORAGE PROT 5-AE
+LOAD B GATE B26
-PAR ERR 5-M
T5 A35
X5 A38
RUN A48
X7 B46
CHECK STOP SW B39
PGM STOP SW BQ1
IMM STOP SW BQ3
START SW BQ2
RESET SW BQ6
LD IAR SW A58
LD STG SW AQ9
LD ACC SW A10
DISPLAY SW A12
PGM LD SW A13
CON INT SW A15
SW CTL RESET A40
ENAB IMM STOP RESET B16
SPARE B42
PWR ON RESET B15
SS MODE A21
I/F PROG LD BUSY A46
2-AE I1 CYCLE (-)
A33 OP CHECK
A31 OP CHECK
5-L + LOAD B GATE
A55 SP CHECK
A53 SP CHECK
B40 CS ERROR CK STP
A49 PARITY CHECK
A47 PARITY CHECK
B24 CMP CHECK
B36 ERROR CK
B18 STOP
B13 IMM STOP
5-AD X7 +
B21 PROGRAM STOP
4-A +START
4-D -LOAD IAR
4-H 5-H -DC RESET
4-C +LOAD STG
4-F -LOAD ACC
4-B +DISPLAY
A29 CONSOLE INT
2-R -1800 STOP
A26 DC RESET P2
B17 DC RESET P1
B10 DC RESET
A57 I/O PROG LOAD
A54 START REQ P1
COMPUTER HARDWARE INC
SC 2154 J
SHEET 3 OF 5


KEY F
E
D
C
B
A
9
8
7
6
5
4
3
2
1
KEY Ø
BQ5
BQ4
A61
A62
A60
A23
A28
A59
A17
A11
A14
AQ7
AQ8
A18
A22
A19
Ø5 R
Ø1 R
Ø4
Ø9
GS
A1
A2
A0
E1
EO
2 WEIGHT
4 WEIGHT
1 WEIGHT
28
31
49
44
43
27
20
19
CG 10mf
R13 5.1K
+5
VG
CB .002 mf CER
A52 + KEY REG DATA
A51 + KEY ACTIVE
A44 + KEY DATA CLOCK
CONSOLE MODE SW A16
PHASA A32
T2 B12 +
+START 3-A
CG1 .01mf
+DISPLAY 3-B
+LOAD STG 3-C
-LOAD IAR 3-D
-LOAD ACC 3-F
RUN MODE B11
+CLEAR SP MODE 2-S
CLEAR STOR SW L45
-DC RESET P2 3-H
Ø7
Ø6
42
34
26
23
21
B37 - COPS/CLEAR
B35 + START CLOCK
B32 - COPS DISP CYCLE
B34 - COPS LOAD CYCLE
B14 - GATE HEX TO B
A43 - GATE HEX TO BUS
A27 - GATE HEX TO IAR
A24 - CLEAR BUS T7
BQ9 - GATE DES TO BUS
A25 - GATE HEX TO ACC
F-J (+) CLEAR MODE
A36 - CLEAR MODE
COMPUTER HARDWARE INC
SC
2154
SHEET 4 OF 5
J


GATE GP7 TO LAMPS
GATE SP TO LAMPS
OP BIT 15
STS E
EM 1800
MD BIT 16
WSPB SW
+CLEAR MODE
OP BIT Ø9
T1
+SYS CP REF P2
MD BIT 17
INT INH PAR CK
X7+
B REG PAR ODD
TØ
XØ
-DC RESET P2
+LOAD B GATE
T3
X3
GATE STAT TO B
STORAGE PROT
LAMP BUS 17
CD BIT 16
-PAR ERR
LAMP BUS 16
LAMP BUS 7
XØ STB
TO XØ RESET
CLOCK B 8-15
GATE STG TO B+
CLOCK B Ø-7
GATE STG TO B
COMPUTER HARDWARE INC
SC
2154
J

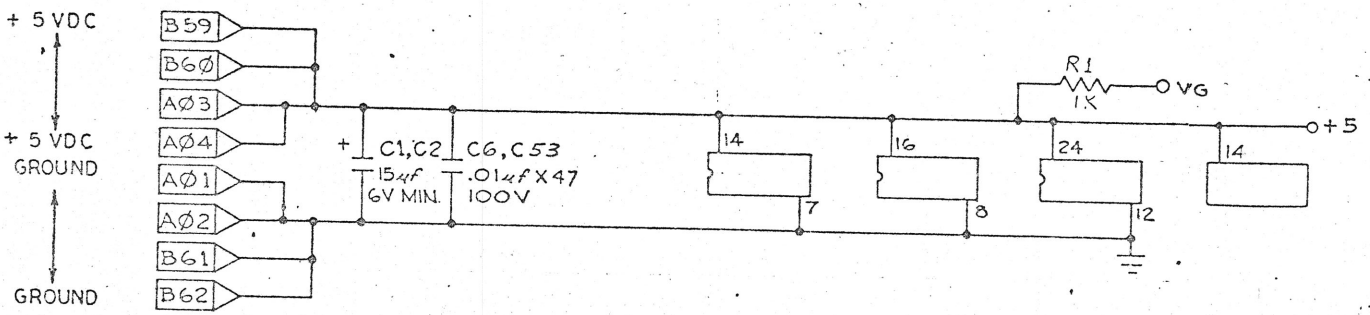
NOTES:
1- DELETED.

57	7474	7474	74148	7474			7400	7474	64
49	7402	7402	7402		7474			7474	56
41	7400	7474	7410	74175	74175	7400	7405	74502	48
33	7474	74148	7474	7402	7410	7438	34A 3324	7474	40
25	7474	7442	7474	7402	7486	7427	7474	7405	32
17	7404	7430	7400	7410	74175	7404	7400	7474	24
9	7403	74161	7404	74500	9602		74161	7402	16
1	74154		7403	74504	7474	7474	7400	7400	8

A1 A61 B1 B61

ASSEMBLY REVISION DATA (REF)

REV. LTR.	DESCRIPTION	REASON
NC1	ADDED CONFIGURATION TABLE	ESTABLISH CONFIGURATION CONTROL
D	ADDED IC INPDS 63	
E	ELEMINATE BUS BAR AND 17 .01uf CAP IMPLEMENT USE OF REV A PC CARD	RELFLECT USE OF MULTILAYER PC CARD
F	CORRECT LAYOUT ERROR ON REV A PC CARD	
G	IMPLEMENT USE OF REV B PC CARD	
H	RELOCATED CAP ITEM 33 TO PROPER LOCATION BELOW IC 42	DRAFTING ERROR
J	ITEM 27, 39pf CAP WAS 47pf CAP	CORRECT MFR. STRIP WIDTH
K	ADD (1) CLOCK MASK AND LSTTL BUFF CIRCUIT	PREVENT SPURIOUS SET OF INT. REQ. BY CYCLE STEAL



CONFIGURATION TABLE		
SC-2157	PC-2158	AC-2159
REV	REV	REV
E	B	J
F	B	K

CONFIGURATION TABLE					
SCHEMATIC	REV	PC	REV	ASSY	REV
SC-2157	NC	PC-2158	NC	AC-2159	NC
SC-2157	NC	PC-2158	NC	AC-2159	A
"	A	"	NC	" "	B
"	M	"	NC	"	C
"	C	"	NC	"	D
"	D	"	A	"	E
"	D	"	A	"	F
"	D	"	B	"	G
"	D	"	B	"	H

LAST USED TABLE	
CODE	REF DES.
SM	R3
	C68

FILE NUMBER

QTY. REQD	PART OR FILE NUMBER	NOMENCLATURE	MFG PART NO OR MATERIAL	MFG NAME OR SPECIFICATION	ITEM NO
		LIST OF MATERIALS			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DIMENSION TOLERANCES
ANGULAR DIMENSION ± 1°
DECIMAL 2 PLACE ± .020
DECIMAL 3 PLACE ± .010
BREAK SHARP EDGES MAX
INSIDE CORNERS MAX
ALL MACHINE SURFACES
CHAMFER ALL THREADS (EXCEPT FULL THREAD INTERFACE)
DO NOT SCALE THIS PRINT

U.ITEM	DWN	CHK	DATE
F		AP	5/19/75
CHANGE RECORD NO	2157		

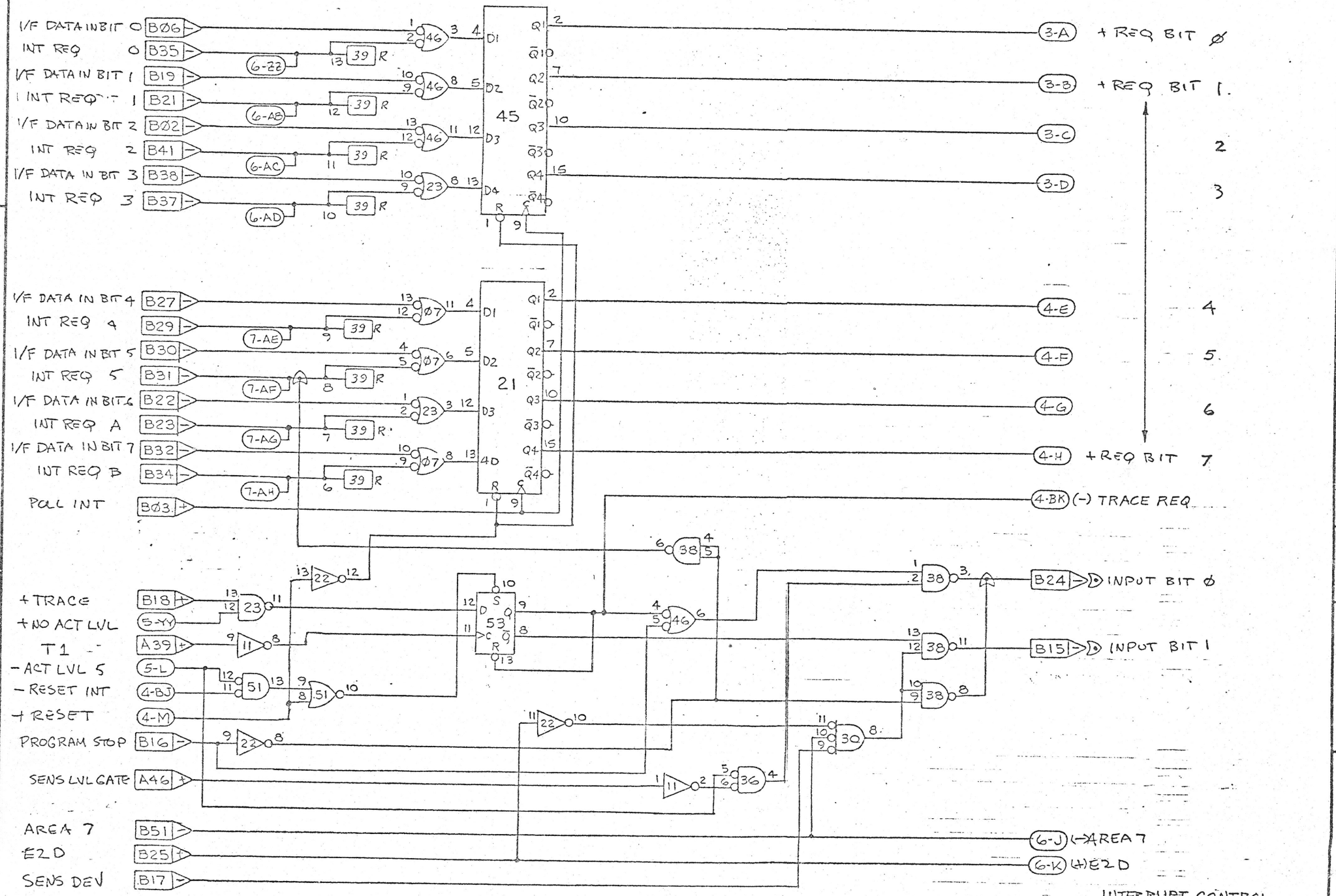
TITLE: CONTROL, INTERRUPT-2131

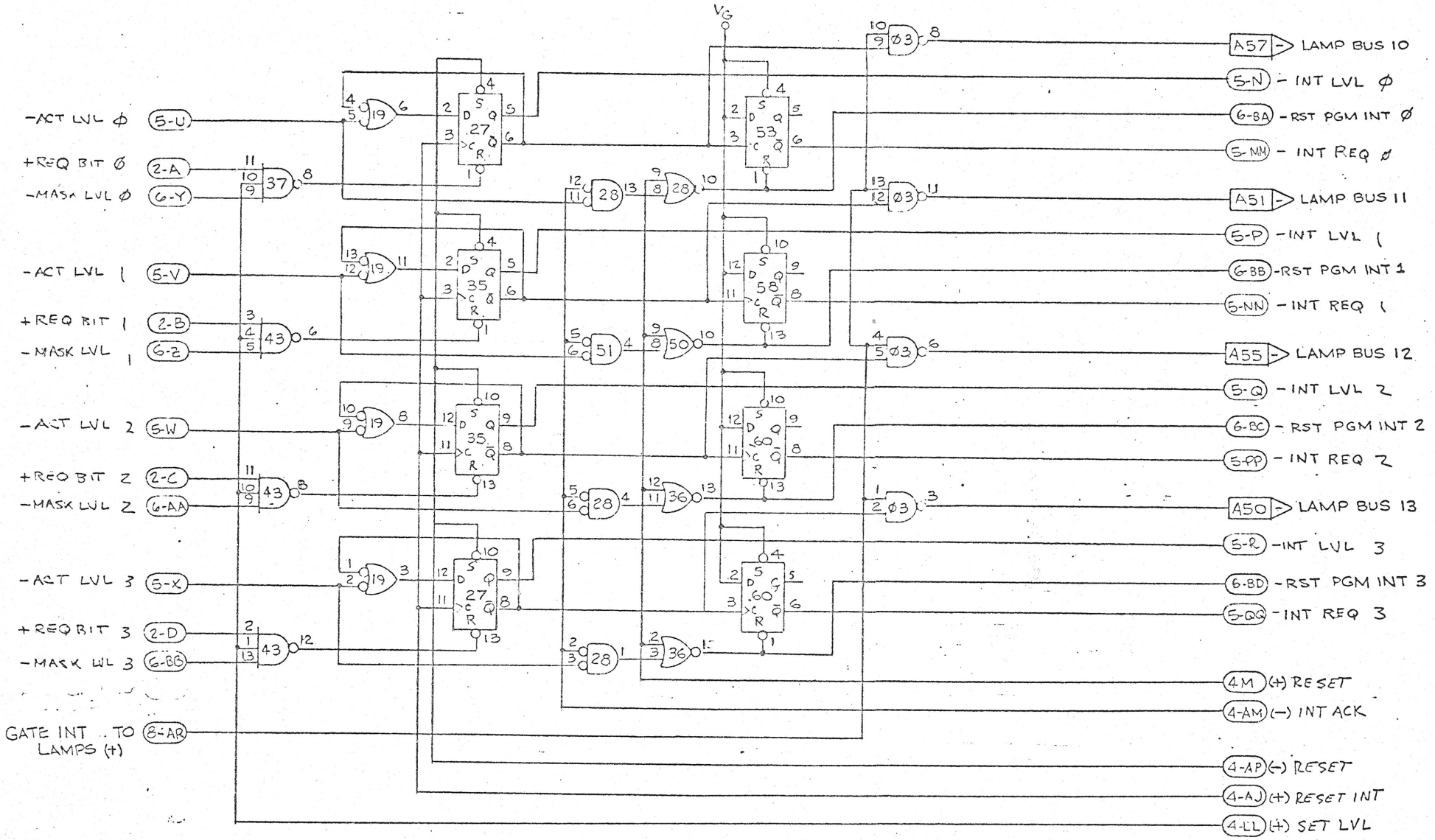
COMPUTER HARDWARE INC.

DRAWN	A FREDELL	CHECKED	AP 5-21-75
DESIGN	T. WALTERS	TYPE-SIZE	SC
SCALE		DWG NO	2157
		SHEET	1 of 2
		REV LET	F

SC2157 B

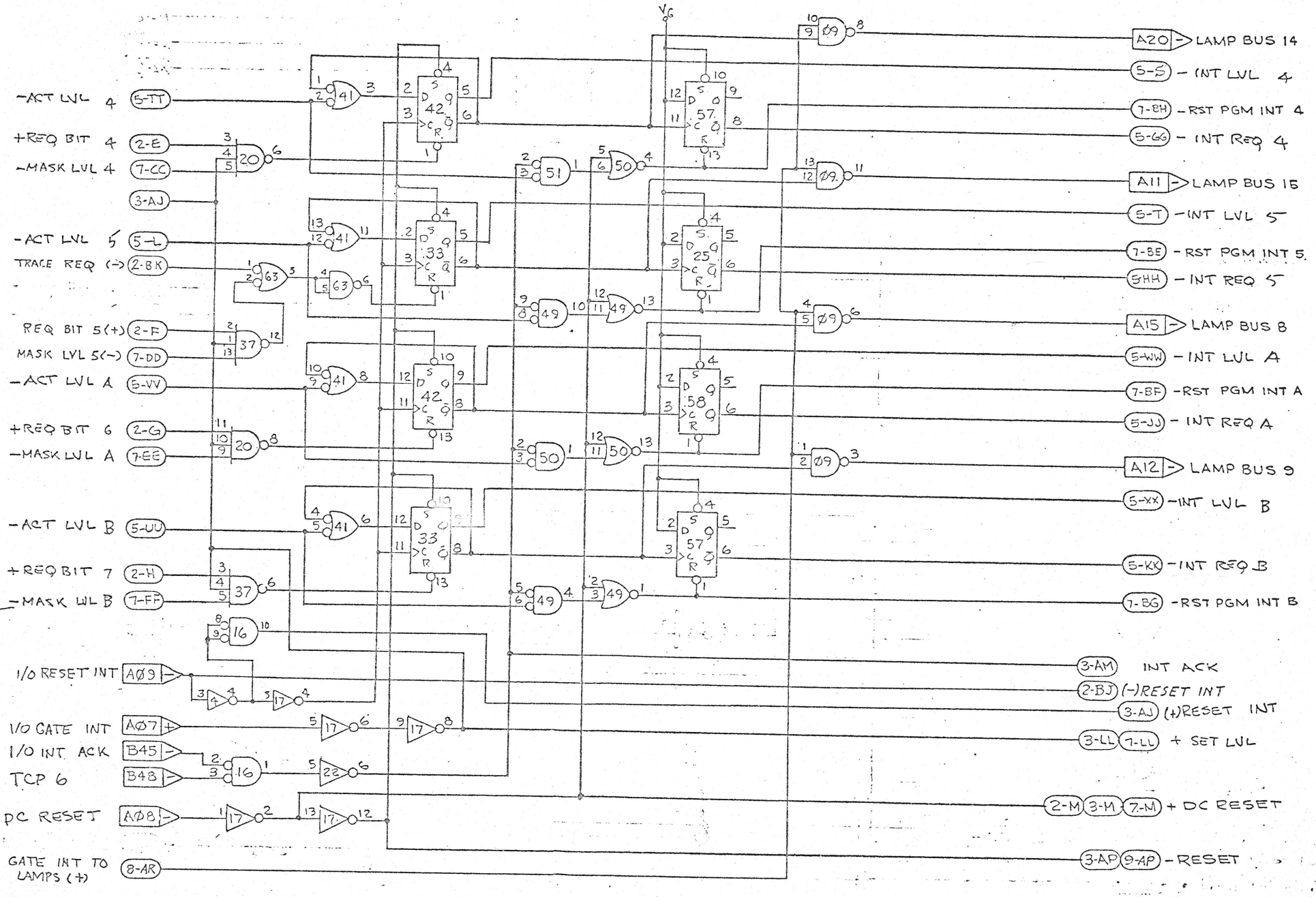
9602 A


I/F DATA IN BIT 0
B06
INT REQ 0
B35
I/F DATA IN BIT 1
B19
INT REQ 1
B21
I/F DATA IN BIT 2
B02
INT REQ 2
B41
I/F DATA IN BIT 3
B38
INT REQ 3
B37
6-AA
6-AB
6-AC
6-AD
39 R
46
23
45
D1
D2
D3
D4
Q1
Q2
Q3
Q4
3-A + REQ BIT Ø
3-B + REQ BIT 1
3-C 2
3-D 3
I/F DATA IN BIT 4
B27
INT REQ 4
B29
I/F DATA IN BIT 5
B30
INT REQ 5
B31
I/F DATA IN BIT 6
B22
INT REQ A
B23
I/F DATA IN BIT 7
B32
INT REQ B
B34
POLL INT
B03
7-AE
7-AF
7-AG
7-AH
Ø7
21
4-E 4
4-F 5
4-G 6
4-H + REQ BIT 7
4-BK (-) TRACE REQ
+TRACE
B18
+NO ACT LVL
5-YY
T1
A39
-ACT LVL 5
5-L
-RESET INT
4-BJ
+RESET
4-M
PROGRAM STOP
B16
SENS LVL GATE
A46
22
53
51
38
30
36
B24 INPUT BIT Ø
B15 INPUT BIT 1
AREA 7
B51
E2D
B25
SENS DEV
B17
6-J AREA 7
6-K E2D
INTERRUPT CONTROL
COMPUTER HARDWARE INC
TYPE-SIZE SC
DWG NO 2157
SHEET 2 OF 9
REV LET F



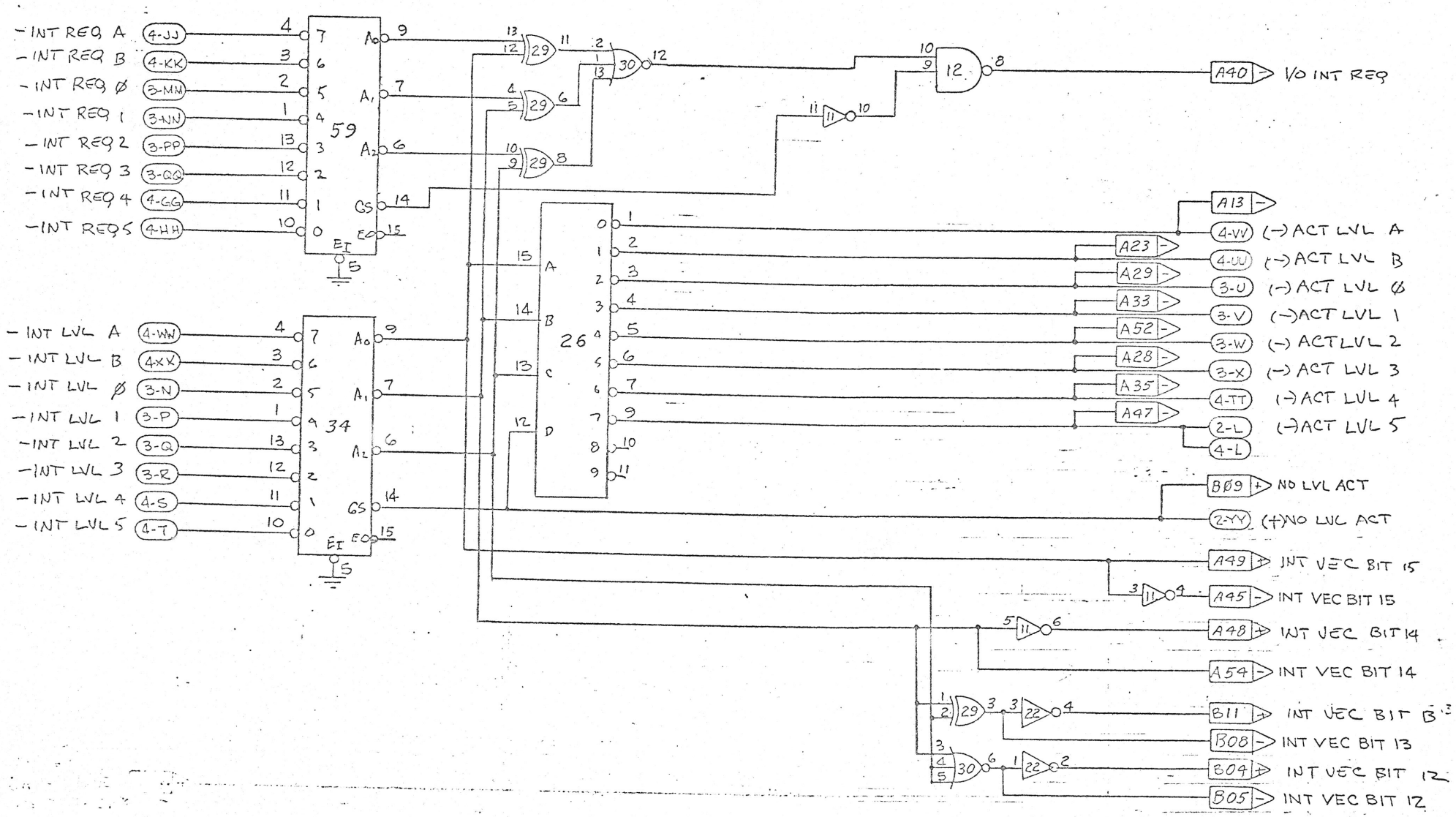
INTERRUPT CONTROL

X COMPUTER HARDWARE INC			
SIZE SC	DWG NO 2157	SHEET 3 OF 9	REV LET F



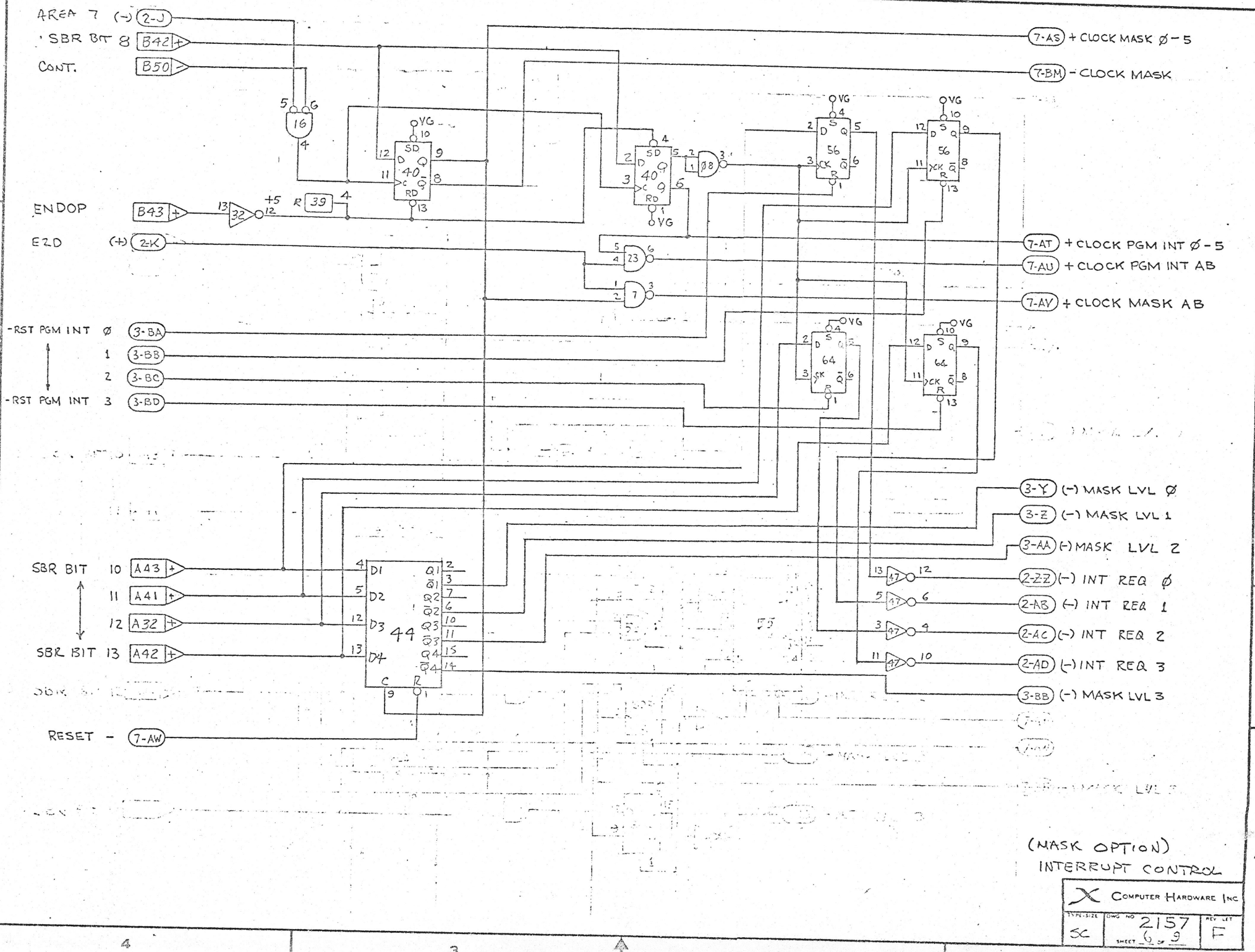
INTERRUPT CONTROL

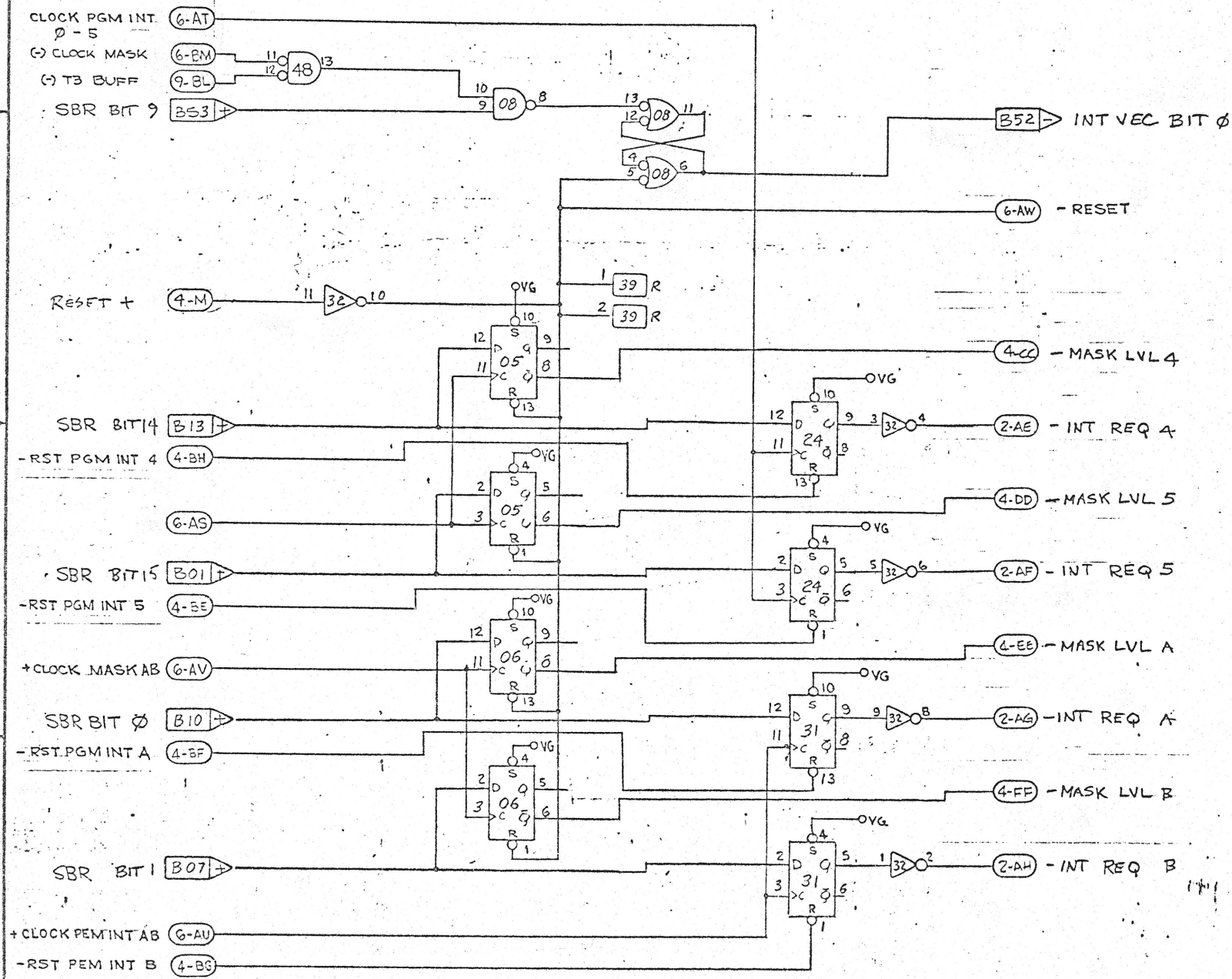
COMPUTER HARDWARE INC.			
TYPE-SIZE	DWG NO		REV. LET
SC	2157		F
	SHEET 4 OF 9		



INTERRUPT CONTROL

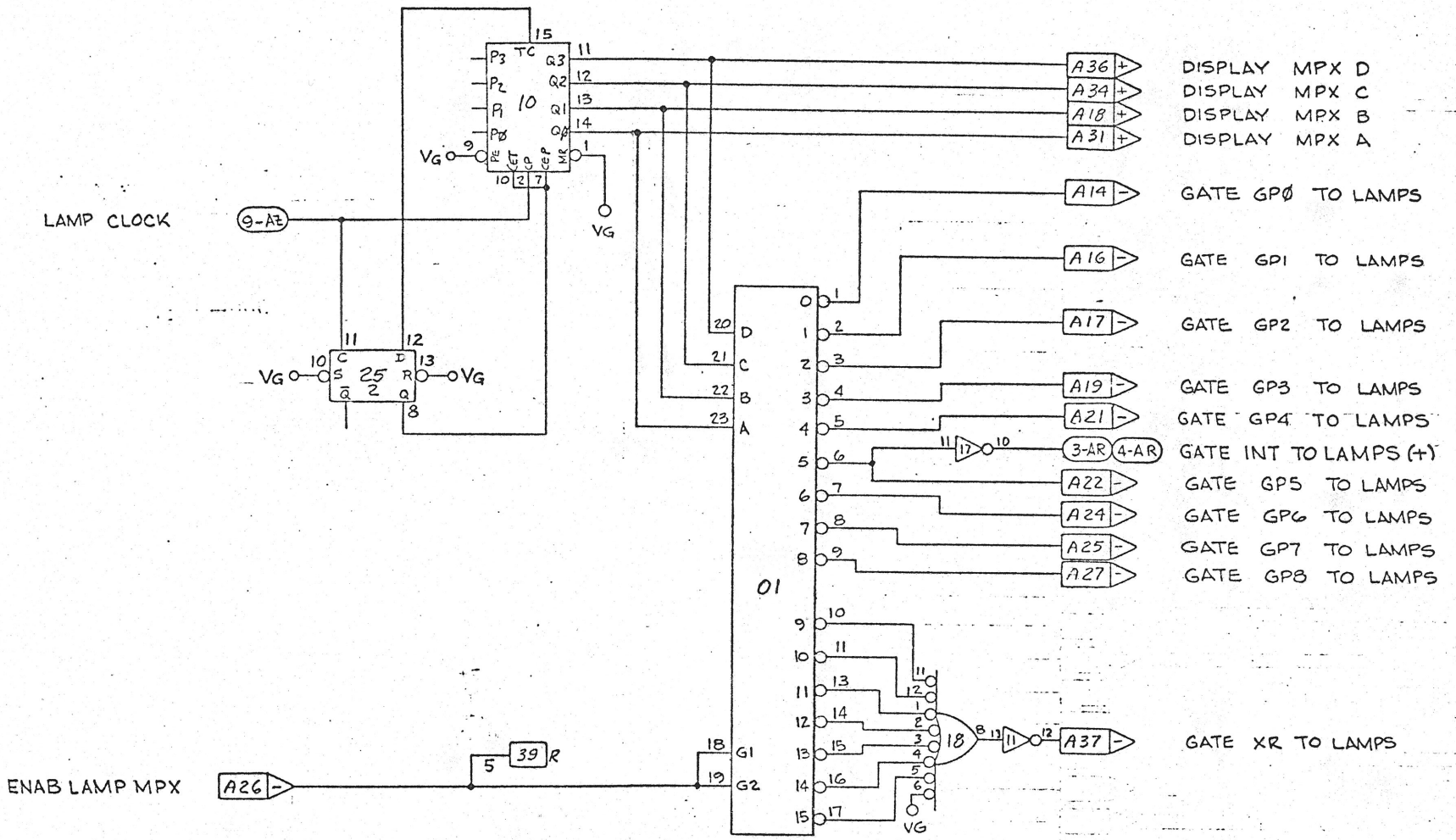
X COMPUTER HARDWARE INC			
TYPE SIZE SC	DWG NO 2157 SHEET 5 of 9	REV LET F	


AREA 7 (-) 2-J
SBR BIT 8 B42 +
CONT. B50 -
ENDOP B43 +
E2D (+) 2-K
-RST PGM INT Ø 3-BA
1 3-BB
2 3-BC
-RST PGM INT 3 3-BD
SBR BIT 10 A43 +
11 A41 +
12 A32 +
SBR BIT 13 A42 +
RESET - 7-AW
7-AS + CLOCK MASK Ø-5
7-BM - CLOCK MASK
7-AT + CLOCK PGM INT Ø-5
7-AU + CLOCK PGM INT AB
7-AV + CLOCK MASK AB
3-Y (-) MASK LVL Ø
3-Z (-) MASK LVL 1
3-AA (-) MASK LVL 2
2-ZZ (-) INT REQ Ø
2-AB (-) INT REQ 1
2-AC (-) INT REQ 2
2-AD (-) INT REQ 3
3-BB (-) MASK LVL 3
(MASK OPTION)
INTERRUPT CONTROL
COMPUTER HARDWARE INC
SIZE SC
DWG NO 2157
SHEET 6 OF 9
REV LET F

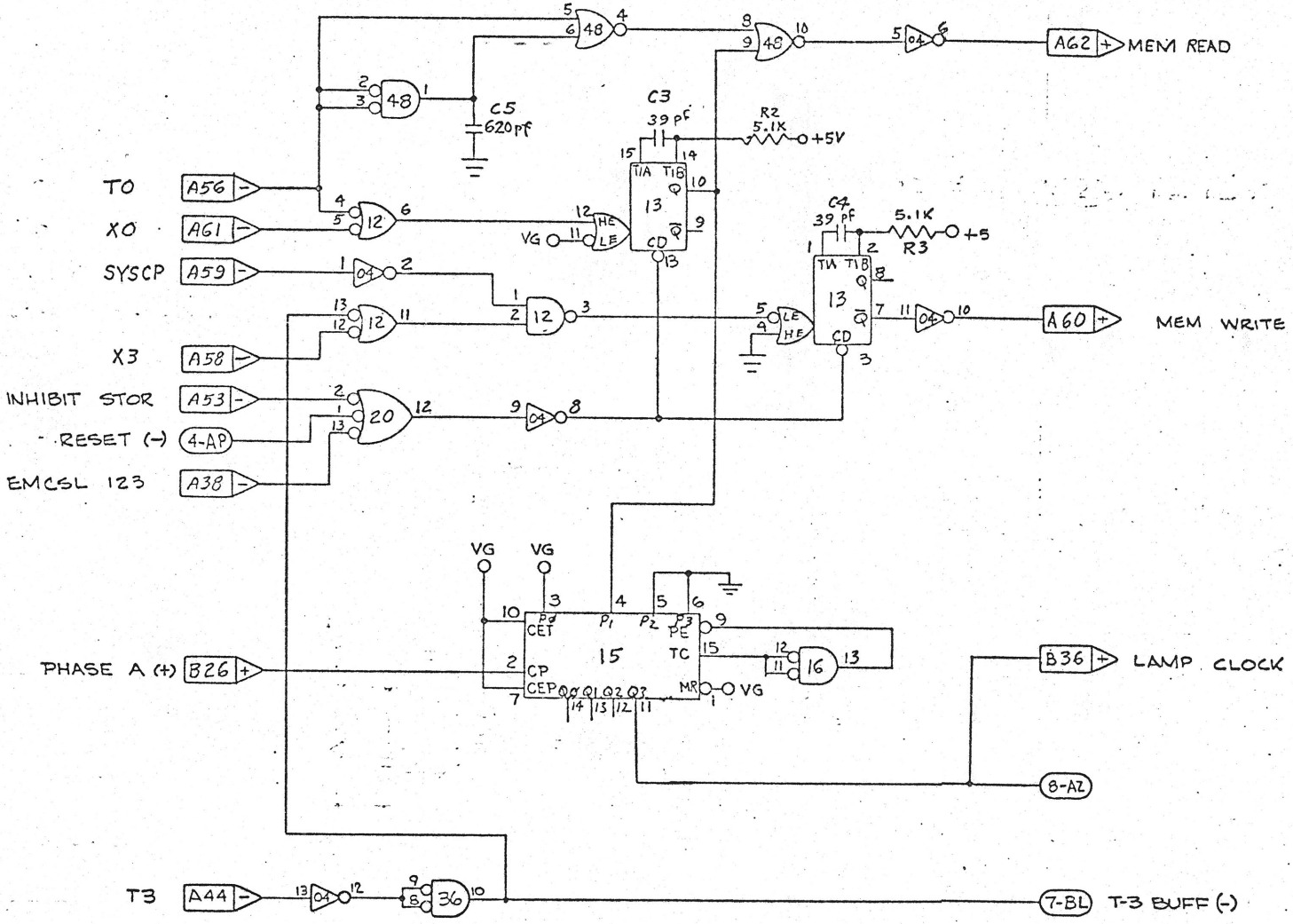


(MASK OPTION)
INTERRUPT CONTROL

X COMPUTER HARDWARE INC		
TYPE SIZE SC	DWG NO 2157 SHEET 7 OF 9	REV LTR F



X COMPUTER HARDWARE INC.			
TYPE-SIZE SC	DWG NO 2157 SHEET 8 OF 9	REV LET F	



Computer Hardware Inc			
TYPE-SIZE SC	DWG NO 2157 SHEET 9 OF 9	REV LET F	

SIGNAL		CONNECTIONS
AC PWR ON RESET	XX -	B18-40,
ACC = 0	10 -	A10-62, A15-49,
ACC BIT 0	10 +	A10-48, A13-11, B08-1, B15-4,
ACC BIT 0 SERIAL IN	15 +	A10-29, A15-58,
ACC BIT 1	10 +	A10-53, A13-38, B08-3, B15-58,
ACC BIT 2	10 +	A10-25, B08-6,
ACC BIT 3	10 +	A10-43, B08-8,
ACC BIT 4	10 +	A10-37, B08-31,
ACC BIT 5	10 +	A10-60, B08-36,
ACC BIT 6	10 +	A10-15, B08-13,
ACC BIT 7	10 +	A10-17, B08-16,
ACC BIT 8	10 +	B09-19, B10-7,
ACC BIT 9	10 +	B09-14, B10-9,
ACC BIT 0 = DRG BIT 0	13 -	A13-12, B15-24,
ACC BIT 10	10 +	B09-3, B10-11,
ACC BIT 11	10 +	B09-5, B10-13,
ACC BIT 12	10 +	B09-13, B10-23,
ACC BIT 13	10 +	B09-16, B10-31,
ACC BIT 14	10 +	B09-1, B10-6,
ACC BIT 15	10 +	A15-15, B09-12, B10-41,
ACC BIT 15 SERIAL IN	15 +	B10-2, B15-30,
ACC S0	15 +	A10-42, A15-39,
ACC S1	15 +	A10-39, A15-53,
ACT LVL A	20 -	A18-44, A20-13,
ACT LVL B	20 -	A20-23,

SIGNAL		CONNECTIONS
ACT LVL 0	20 -	A20-29,
ACT LVL 1	20 -	A20-33,
ACT LVL 2	20 -	A20-52,
ACT LVL 3	20 -	A20-28,
ACT LVL 4	20 -	A20-35,
ACT LVL 5	20 -	A20-47,
ADDOP	17 +	A15-12, A17-59, B13-48,
ADV CS CLOCK	11 +	A17-26, B08-41, B09-40, B11-13, B12-37, B13-35, B14-44,
ADV IAR GATE	16 +	A09-37, B16-17,
ADV IAR 0-7	9 +	A08-41, A09-14,
ADV TCP	12 +	A12-37, A16-56, A17-42,
ALU = 0	10 -	A13-29, B10-10,
ALU A=B	10 +	A10-41, A13-56,
ALU BIT 0	10 +	A10-26, A13-28, B15-51,
ALU CARRY OUT	13 +	A13-10, B15-45,
ALU CN	13 -	A13-16, B10-15,
ALU CN+4	10 -	A10-27, A13-9,
ALU MODE	15 +	A10-6, A15-50,
ALU OVFL	15 +	B15-27,
ALU SUB	15 +	A13-8, B15-18,
ALU S0	15 +	A10-44, A15-13,
ALU S1	15 +	A10-24, A15-56,
ALU S2	15 +	A10-10, A15-7,
ALU S3	15 +	A10-18, A15-45,
AND	17 -	A15-43, B17-9,

SIGNAL		CONNECTIONS
AREA 0	18 -	B14-23, B18-1,
AREA 7	18 -	A14-45, B18-39, B20-51,
BSC	17 -	A15-32, B13-51, B16-31, B17-16,
BSI	17 -	A17-5, B13-49, B14-34, B15-46, B16-48,
BSIE	17 +	A17-58, B16-6,
BUS BIT 0	+	A08-24, A10-30, A11-38,
BUS BIT 1	+	A08-20, A10-12, A11-33,
BUS BIT 2	+	A08-22, A10-32, A11-36,
BUS BIT 3	+	A08-26, A10-36, A11-31,
BUS BIT 4	+	A08-28, A10-54, A11-19,
BUS BIT 5	+	A08-25, A10-52, A11-14,
BUS BIT 6	+	A08-48, A10-11, A11-17,
BUS BIT 7	+	A08-27, A10-13, A11-12,
BUS BIT 8	+	A09-36, A12-28, B10-16, B13-20,
BUS BIT 9	+	A09-33, A12-29, B10-24, B13-46,
BUS BIT 10	+	A09-26, A12-23, B10-12, B13-24,
BUS BIT 11	+	A09-29, A12-21, B10-18, B13-32,
BUS BIT 12	+	A09-24, B10-4, B12-46, B13-42,
BUS BIT 13	+	A09-23, A12-39, B10-3, B13-37,
BUS BIT 14	+	A09-21, B10-8, B12-53, B13-33,
BUS BIT 15	+	A09-20, A12-19, B10-5, B13-39,
CARRY	13 -	A15-60, B13-1,
CARRY TO ALU	15 +	A13-14, A15-37,
CCC = 0	13 -	A16-33, B13-30, B15-41, B17-15,
CCC = 1	13 -	A15-28, A17-34, B13-25, B16-57,

SIGNAL		CONNECTIONS
CD BIT 0	8 -	A08-50, A21-26,
CD BIT 1	8 -	A08-45, A21-28,
CD BIT 2	8 -	A08-43, A21-30,
CD BIT 3	8 -	A08-57, A21-32,
CD BIT 4	8 -	A08-53, A21-34,
CD BIT 5	8 -	A08-55, A21-36,
CD BIT 6	8 -	A08-51, A21-38,
CD BIT 7	8 -	A08-49, A21-40,
CD BIT 8	9 -	A09-61, A21-42,
CD BIT 9	9 -	A09-57, A21-44,
CD BIT 10	9 -	A09-52, A21-46,
CD BIT 11	9 -	A09-54, A21-48,
CD BIT 12	9 -	A09-49, A21-50,
CD BIT 13	9 -	A09-17, A21-52,
CD BIT 14	9 -	A09-55, A21-54,
CD BIT 15	9 -	A09-51, A21-56,
CD BIT 16	11 -	A21-58, B11-49,
CD BIT 17	12 -	A12-54, A21-60,
CES 8	XX -	A14-16,
CES 9	XX -	A14-28,
CES 10	XX -	A14-5,
CES 11	XX -	A14-22,
CES 12	XX -	A14-56,
CES 13	XX -	B14-5,
CES 14	XX -	B14-8,

SIGNAL		CONNECTIONS
CES 15	XX -	B14-18,
CHECK STOP S-111	22 -	A18-10, A22-43, B19-39,
CLEAR BUS T7	19 -	A19-24, B16-36,
CLEAR MODE	19 -	A19-36,
CLEAR STG S-304	22 -	A19-45, B22-23,
CLOCK SBR 0- 7	19 +	A08-46, B19-23,
CLOCK SBR 8-15	19 +	A09-56, B19-28,
CMP CHK	17 -	A17-6, B19-24,
CMP CHK IND	17 -	A17-28, B22-49,
CMPOP	17 +	A13-30, A15-44, A17-62, B16-53,
COMP EQUAL	13 +	A13-61, B16-8,
COMP EQUAL	13 -	A13-57,
COMP LESS OR EQUAL	13 +	A13-37, B16-22,
COND RUN	17 +	A17-50, B19-45,
CONS INT S-310	22 -	A19-15, B22-34,
CONSOLE INT	19 -	A19-29,
CONSOLE S-112	22 -	A17-25, A19-16, B22-15,
CONTROL	18 -	B18-28, B20-50,
COPS DISP CYCLE	19 -	B17-52, B19-32,
COPS LOAD CYCLE	19 -	B19-34,
COPS+CLEAR	19 -	B11-55, B14-49, B15-6, B16-1, B17-11, B19-37,
CPU CLOCK	17 -	A18-27, B17-22,
CS ERR CHK STP	19 -	B11-45, B19-40,
CS HOLD T7	11 -	A11-37, B12-34,
CS LEVEL	11 +	A18-34, B11-19, B17-20,

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SIGNAL		CONNECTIONS
CS LEVEL	11 -	A15-5, A16-47, B11-16,
CS REQUEST	18 +	B11-42, B18-20,
DBL PREC OP	17 +	A13-54, A15-10, A17-47, B16-14,
DC RESET	19 +	A08-11, A09-10, A17-24, B11-24, B19-10,
DC RESET P1	19 -	B13-5, B14-45, B16-43, B19-17,
DC RESET P2	19 -	A19-26, A20-8, B18-33,
DES 0	22 -	A14-14, B22-24,
DES 1	22 -	A14-19, B22-26,
DES 2	22 -	A14-21, A22-26,
DES 3	22 -	A14-9, A22-28,
DES 4	22 -	A14-53, A22-30,
DES 5	22 -	A14-46, A22-32,
DES 6	22 -	A14-44, A22-34,
DES 7	22 -	A14-49, A22-36,
DES 8	22 -	A14-25, A22-38,
DES 9	22 -	A14-36, A22-40,
DES 10	22 -	A14-6, A22-42,
DES 11	22 -	A14-12, A22-44,
DES 12	22 -	B14-1, B22-3,
DES 13	22 -	B14-4, B22-1,
DES 14	22 -	B14-7, B22-2,
DES 15	22 -	B14-19, B22-4,
DIFF SIGN	13 +	A13-33, B15-33,
DIFF SIGN	13 -	A13-22,
DIOP	17 -	A16-5, B17-17,

SIGNAL		CONNECTIONS
DISP STG S-303	22 -	A19-12, B22-31,
DISP/SP S-112	22 -	A22-51, B19-31,
DIV	17 -	B13-21, B15-13, B17-1,
DIV CMP HOLD T7	13 +	B13-17, B16-19,
DIV CMP HOLD T7	13 -	A17-33, B12-25, B13-15,
DIV E	15 +	A16-36, B13-6, B15-23,
DIV E1	15 +	A13-23, B15-11,
DIV OVFL RST CCC	15 +	B13-34, B15-34,
DRG = 0	10 -	A13-40, B10-17, B15-44,
DRG BIT 0	10 +	A10-46, A13-7, B15-31,
DSR CLOCK	XX +	B08-14, B09-36,
DXFR	18 +	B14-22, B18-15,
E CYCLES	17 -	A13-60, A15-48, A17-36, B16-32,
EMCSL 123	9 -	A16-38, A20-38, B09-35, B15-19,
ENAB IXR P1	8 +	B08-12, B09-29,
ENAB IXR P2	8 +	B08-53, B09-31,
ENAB LAMP MPX	XX -	A20-2, A20-26,
ENAB SAR BIT 0	14 +	B08-22, B14-39,
END OP	17 +	A17-7, A18-25, B14-25, B20-43,
ENDOP EARLY	17 +	B14-46, B17-14, B19-55,
ENOP 1	XX +	A19-41,
ENOP 2	XX +	B18-17,
ENOP 3	XX -	A09-41,
ENOP 4	XX +	A14-23,
ENOP 5	XX +	B19-16,

SIGNAL		CONNECTIONS
ENOP 6	XX -	B14-30,
EOR	17 -	B15-1, B17-4,
ERROR CHK	19 -	A12-15, B14-28, B19-36,
EXT BIT 0	10 +	A15-6, B10-1,
EXT BIT 14	10 +	A13-34, B10-50,
EXT BIT 15	10 +	A13-6, B10-49, B15-12,
EXT BIT 15 SERIAL IN	15 +	B10-34, B15-17,
EXT S0	15 +	A10-58, A15-54,
EXT S1	15 +	A10-56, A15-55,
E1 CYCLE	17 -	A13-27, A17-12, B15-7, B16-41, B18-22,
E2 CYCLE	17 +	A11-50, A15-8, A16-50, A17-30, B13-41, B18-38,
E2 DXFR	18 +	B14-26, B18-21, B20-25,
E3 CYCLE	17 +	B11-7, B16-49, B17-46, B18-18,
E3 DXFR	18 +	B14-24, B18-23,
FLT	17 -	B17-3,
GATE ACC TO BUS	16 -	A16-29, B10-14,
GATE ALU TO ACC	16 -	A15-31, B16-24,
GATE ALU TO BUS	16 -	A10-59, B16-42,
GATE CCC TO IXR	13 +	B13-29,
GATE CCC TO IXR	13 -	A13-53, A16-60,
GATE DES TO I/O	19 -	A14-20, B17-39, B19-9,
GATE DISP TO DRG	16 -	A11-49, A16-16, B12-9,
GATE DISP TO TAC	16 -	A11-47, A16-9, B12-11,
GATE DIV OVFL T7	13 +	B13-45, B15-40,
GATE DSR TO BUS	XX -	B08-23, B09-44,

SIGNAL		CONNECTIONS
GATE EXT TO ACC	16 -	A15-26, A16-49,
GATE EXT TO BUS	16 -	B10-19, B16-9,
GATE I/O TO BUS	12 -	A12-16, B11-44,
GATE I/O TO DRG	17 -	A12-14, A16-13, A17-54,
GATE I/O TO SBR	17 -	A12-10, A16-39, B17-55,
GATE I/O TO SBR + ACC	16 -	A12-11, A15-29, A16-26,
GATE IAR TO BUS	16 -	B08-47, B09-56, B16-44,
GATE ILSW	18 +	A18-30, A20-46,
GATE INT	17 +	A17-52, A20-7,
GATE IXR TO BUS	16 -	A11-28, A12-42, A16-55,
GATE IXR TO CCC	13 -	A13-32, A16-15,
GATE IXR TO OPR	15 -	A16-19, B11-21, B12-36, B15-15,
GATE KDR TO ACC	19 +	A15-27, A19-25,
GATE KDR TO BUS	19 -	A19-43, B08-29, B09-42,
GATE KDR TO IAR	19 -	A19-27, B16-5,
GATE KDR TO SBR	19 -	A16-32, B19-14,
GATE LAMPS P0	20 -	A08-9, A09-9, A20-14,
GATE LAMPS P1	20 -	A08-16, A09-16, A20-16, B19-48,
GATE LAMPS P2	20 -	A08-10, A09-11, A20-17, B13-40,
GATE LAMPS P3	20 -	A11-61, A12-35, A20-19,
GATE LAMPS P4	20 -	A08-15, A09-15, A20-21,
GATE LAMPS P5	20 -	A20-22, B13-43,
GATE LAMPS P6	20 -	A11-59, A12-33, A20-24,
GATE LAMPS P7	20 -	A12-31, A20-25, B17-25, B19-44,
GATE LAMPS P8	20 -	A20-27, B10-37,

SIGNAL		CONNECTIONS
GATE LAMPS P9-F	20 -	A11-62, A12-32, A20-37,
GATE MAR TO BUS	16 -	A16-54, B08-27, B09-57,
GATE MD TO DRG 0- 7	16 -	A10-23, A16-30,
GATE MD TO DRG 8-15	16 -	B10-43, B16-20,
GATE MD TO OPR	15 +	A15-23, B11-35, B12-31,
GATE MD TO SBR	19 +	A08-60, A09-45, A19-5,
GATE SBR TO BUS	15 -	B08-30, B09-51, B15-53,
GATE SBR TO CCC	13 -	A13-41, B15-42,
GATE SBR TO IXR P1	16 -	B15-55, B16-40,
GATE SBR TO IXR P2	16 -	A16-58, B15-56,
GATE STAT TO SBR	16 -	A08-17, A16-37, B13-55, B19-38,
GEN ADD BIT 15	17 +	A17-27, B09-39,
HEX BIT 0	8 +	A22-5, B08-2,
HEX BIT 1	8 +	A22-17, B08-24,
HEX BIT 2	8 +	A22-7, B08-5,
HEX BIT 3	8 +	A22-15, B08-7,
HEX BIT 4	8 +	B08-33, B22-57,
HEX BIT 5	8 +	A22-21, B08-35,
HEX BIT 6	8 +	B08-15, B22-58,
HEX BIT 7	8 +	A22-9, B08-17,
HEX BIT 8	9 +	A22-25, B09-11,
HEX BIT 9	9 +	B09-18, B22-55,
HEX BIT 10	9 +	A22-23, B09-2,
HEX BIT 11	9 +	A22-13, B09-4,
HEX BIT 12	9 +	B09-15, B22-51,

SIGNAL		CONNECTIONS
HEX BIT 13	9 +	A22-27, B09-17,
HEX BIT 14	9 +	B09-6, B22-53,
HEX BIT 15	9 +	A22-11, B09-8,
HEXD ENAB	17 -	A22-19, B17-28,
HOLD CS ADD (X7)	11 +	B08-58, B09-46, B11-23,
I/F BLOCK CLOCK	21 -	A18-26, B11-51, B21-7,
I/F CLOCK	18 -	B18-53, B21-17,
I/F CPU CLOCK	18 +	A18-31, B21-18,
I/F CS CYCLE	18 -	A18-40, B21-21,
I/F CS DATA STORE	21 -	A18-5, B17-50, B21-26,
I/F CS REQ	21 -	A18-37, B21-8,
I/F DC RESET	18 -	B18-48, B21-4,
I/F DXFR	18 -	B18-19, B21-42,
I/F E1+E3	18 +	A18-58, B21-19,
I/F E2+E3	18 +	A18-51, B21-16,
I/F FUNC CLEAR	18 -	A18-32, B21-36,
I/F IN BIT 0	-	A14-15, A18-29, B20-6, B20-24, B21-12,
I/F IN BIT 1	-	A14-17, A18-39, B20-15, B20-19, B21-2,
I/F IN BIT 2	-	A14-38, A18-28, B20-2, B21-9,
I/F IN BIT 3	-	A14-39, B20-38, B21-13,
I/F IN BIT 4	-	A14-55, B20-27, B21-15,
I/F IN BIT 5	-	A14-58, B20-30, B21-5,
I/F IN BIT 6	-	B14-20, B20-22, B21-11,
I/F IN BIT 7	-	A14-57, B20-32, B21-49,
I/F IN BIT 8	-	A14-8, B21-48,

SIGNAL		CONNECTIONS
I/F IN BIT 9	-	A14-47, B21-27,
I/F IN BIT 10	-	A14-10, B21-33,
I/F IN BIT 11	-	A14-24, B21-35,
I/F IN BIT 12	-	B14-3, B21-53,
I/F IN BIT 13	-	B14-6, B21-51,
I/F IN BIT 14	-	B14-21, B21-47,
I/F IN BIT 15	-	B14-11, B21-29,
I/F INH CS REQ	18 +	A18-19, B21-24,
I/F OUT BIT 0	18 -	B18-14, B21-22,
I/F OUT BIT 1	18 -	A18-57, B21-1,
I/F OUT BIT 2	18 -	B18-3, B21-55,
I/F OUT BIT 3	18 -	A18-7, B21-32,
I/F OUT BIT 4	18 -	B18-16, B21-28,
I/F OUT BIT 5	18 -	A18-20, B21-34,
I/F OUT BIT 6	18 -	B18-51, B21-40,
I/F OUT BIT 7	18 -	A18-14, B21-38,
I/F OUT BIT 8	18 -	B18-47, B21-25,
I/F OUT BIT 9	18 -	A18-61, B21-20,
I/F OUT BIT 10	18 -	B18-13, B21-31,
I/F OUT BIT 11	18 -	A18-35, B21-23,
I/F OUT BIT 12	18 -	B18-10, B21-41,
I/F OUT BIT 13	18 -	A18-18, B21-56,
I/F OUT BIT 14	18 -	B18-9, B21-44,
I/F OUT BIT 15	18 -	A18-38, B21-45,
I/F PARITY ERR	18 -	A18-55, B21-37,

SIGNAL		CONNECTIONS
I/F PHASE A	18 -	A18-48, B21-43,
I/F POLL	18 -	B18-6, B21-30,
I/F PROG LOAD	18 -	A18-17, B21-46,
I/F PROG LOAD BUSY	21 -	A18-22, A19-46, B21-6,
I/F PWR ON RST	18 -	A18-6, B21-14,
I/F RESET EXTEND	21 -	A18-23, B21-10,
I/F STG PRT ERR	18 -	A18-11, B21-57,
I/O IN BIT 0	14 +	A11-39, A14-29, B08-54,
I/O IN BIT 1	14 +	A11-30, A14-31, B08-57,
I/O IN BIT 2	14 +	A11-34, A14-35, B08-43,
I/O IN BIT 3	14 +	A11-29, A14-37, B08-46,
I/O IN BIT 4	14 +	A11-16, B08-38, B14-10,
I/O IN BIT 5	14 +	A11-11, A14-34, B08-37,
I/O IN BIT 6	14 +	A11-15, B08-34, B14-17,
I/O IN BIT 7	14 +	A11-10, A14-41, B08-21,
I/O IN BIT 8	14 +	A14-26, B09-55, B12-55,
I/O IN BIT 9	14 +	A14-27, B09-52, B12-44,
I/O IN BIT 10	14 +	A14-33, B09-45, B12-49,
I/O IN BIT 11	14 +	A14-30, B09-48, B12-48,
I/O IN BIT 12	14 +	A14-59, B09-37, B12-52,
I/O IN BIT 13	14 +	B09-32, B12-50, B14-2,
I/O IN BIT 14	14 +	B09-28, B12-51, B14-14,
I/O IN BIT 15	14 +	A14-60, B09-26, B12-45,
IA CYCLE	17 -	A16-42, A17-8,
IAR CARRY 8-15	9 +	A08-37, A09-30,

SIGNAL		CONNECTIONS
IAR CMP S-112	22 -	B17-26, B22-13,
II CYCLE	17 -	A16-46, A17-15,
ILLOPS	17 -	B13-10, B17-13, B19-25,
IMM STOP	19 +	A12-27, B19-13,
IMM STOP S-305	22 -	B19-3, B22-19,
INDST	17 -	A16-28, B17-56,
INH ALU TO ACC	13 +	A13-21, B16-55,
INH CS REQ	XX -	A18-13,
INH INTERRUPT	14 +	A17-46, B14-37,
INH PAR CHK ON INT	17 -	B17-29, B19-56,
INH STOR	17 -	A17-9, A20-53, B09-27,
INT ACK	17 -	A14-61, B17-45, B20-45,
INT BSI I1 I2	17 +	A15-52, A17-37, B16-30,
INT DISABLE S-109	22 -	A22-24, B14-50,
INT REQ	20 -	A17-39, A20-40,
INT REQ A	-	A18-42, B20-23,
INT REQ B	-	B20-34,
INT REQ 0	-	B20-35,
INT REQ 1	-	B20-21,
INT REQ 2	-	B20-41,
INT REQ 3	-	B20-37,
INT REQ 4	-	B20-29,
INT REQ 5	-	B20-31,
INT VEC BIT 0	20 -	A14-11, B20-52,
INT VEC BIT 12	20 +	A18-59, B20-4,

SIGNAL		CONNECTIONS
INT VEC BIT 12	20 -	A14-54, B20-5,
INT VEC BIT 13	20 +	A18-49, B20-11,
INT VEC BIT 13	20 -	B14-16, B20-8,
INT VEC BIT 14	20 +	A18-60, A20-48,
INT VEC BIT 14	20 -	A20-54, B14-9,
INT VEC BIT 15	20 +	A18-46, A20-49,
INT VEC BIT 15	20 -	A14-48, A20-45,
IXR ADD 0	15 +	A11-24, B12-4, B15-48,
IXR ADD 1	15 +	A11-9, A12-5, A15-21,
IXR ADD 2	15 +	A11-8, A12-24, B15-21,
I1 CYCLE	17 -	A15-42, A17-21, B13-22, B16-26, B19-43,
I2 CYCLE	17 -	A17-23, B16-3,
KEY A	22 -	A19-23, B22-45,
KEY ACTIVE	19 +	A17-32, A19-51,
KEY B	22 -	A19-60, B22-47,
KEY C	22 -	A19-62, B22-48,
KEY D	22 -	A19-61, B22-46,
KEY DATA 8	9 +	B08-48, B09-10,
KEY DATA CLOCK	19 +	A19-44, B08-56, B09-23,
KEY E	22 -	B19-4, B22-50,
KEY F	22 -	B19-5, B22-52,
KEY REG DATA	19 +	A19-52, B09-21,
KEY 0	22 -	A19-19, A22-29,
KEY 1	22 -	A19-22, A22-31,
KEY 2	22 -	A19-18, B22-33,

SIGNAL		CONNECTIONS
KEY 3	22 -	A19-8, B22-35,
KEY 4	22 -	A19-7, B22-37,
KEY 5	22 -	A19-14, B22-39,
KEY 6	22 -	A19-11, B22-41,
KEY 7	22 -	A19-17, B22-43,
KEY 8	22 -	A19-59, B22-54,
KEY 9	22 -	A19-28, B22-56,
LAMP BUS 0	-	A08-34, A10-55, A17-17, A22-53, B11-14, B13-54,
LAMP BUS 1	-	A08-36, A10-33, A17-18, A22-48, B11-8, B13-56,
LAMP BUS 2	-	A08-61, A10-40, A17-14, A22-55, B11-1, B13-52,
LAMP BUS 3	-	A08-62, A10-51, A17-19, A22-54, B11-4, B13-58,
LAMP BUS 4	-	A08-5, A10-49, A11-32, A17-11, A22-56, B13-44,
LAMP BUS 5	-	A08-40, A10-57, A11-35, A17-16, A22-46, B13-57,
LAMP BUS 6	-	A08-42, A10-31, B11-15, B22-8,
LAMP BUS 7	-	A08-21, A10-35, A11-56, A22-62, B19-47,
LAMP BUS 8	-	A09-18, A12-30, A20-15, A22-58, B10-27,
LAMP BUS 9	-	A09-7, A12-26, A20-12, B10-33, B22-18,
LAMP BUS 10	-	A09-31, A12-25, A20-57, B10-29, B22-16,
LAMP BUS 11	-	A09-35, A12-34, A20-51, B10-35, B22-12,
LAMP BUS 12	-	A09-22, A12-36, A20-55, B10-48, B22-6,
LAMP BUS 13	-	A09-42, A12-38, A20-50, B10-53, B22-10,
LAMP BUS 14	-	A09-28, A12-40, A20-20, B10-47, B22-14,

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SIGNAL		CONNECTIONS
LAMP BUS 15	-	A09-34, A12-22, A20-11, A22-52, B10-51,
LAMP BUS 16	-	A22-50, B13-47, B19-50,
LAMP BUS 17	-	A22-60, B13-53, B19-52,
LAMP CLOCK	20 +	B20-36, B22-5,
LAMP MPX A	20 +	A11-21, A12-6, A20-31, B22-7,
LAMP MPX B	20 +	A11-25, A12-20, A20-18, B22-22,
LAMP MPX C	20 +	A11-26, A12-41, A20-34, B22-27,
LAMP MPX D	20 +	A20-36, B22-25,
LAST I	17 -	A13-46, A15-61, A17-40, B11-36, B14-57, B16-11,
LAST M	XX +	B13-28,
LDOP	17 +	A17-60, B16-37,
LDS	17 +	A13-42, A15-47, B17-27,
LDX	17 -	A16-43, B14-54, B17-40,
LDX OP BIT 10	14 -	A17-22, B14-36,
LOAD ACC S-309	22 -	A19-10, B22-28,
LOAD DRG GATE	16 +	A10-50, A16-17,
LOAD IAR GATE	16 -	A08-38, A09-40, B16-18,
LOAD IAR S-300	22 -	A19-58, B22-32,
LOAD IXR 0- 7 GATE	16 -	A11-20, B16-16,
LOAD IXR 8-15 GATE	16 -	B12-30, B16-28,
LOAD MAR STB	16 -	A16-57, B08-11, B09-20,
LOAD SBR GATE	16 +	A16-41, B19-26,
LOAD STG S-306	22 -	A19-9, B22-30,
LOAD TAC GATE	16 +	A16-21, B10-26,

SIGNAL		CONNECTIONS
MAR BIT 14	9 +	B09-33, B15-22,
MAR BIT 15	9 +	B09-34, B15-47,
MAR CMP	9 -	A09-62, B17-19,
MAR CMP P1	8 +	B08-9, B09-22,
MAR CMP P2	8 +	B08-55, B09-30,
MAR 4-7 = 0	8 +	B08-52, B09-25,
MD BIT 1	21 -	A08-30, A10-9, A21-29, B11-57,
MD BIT 2	21 -	A08-13, A10-16, A21-31, B11-56,
MD BIT 3	21 -	A08-18, A10-14, A21-33, B11-58,
MD BIT 4	21 -	A08-29, A10-5, A21-35, B11-31,
MD BIT 5	21 -	A08-19, A10-20, A21-37, B11-46,
MD BIT 6	21 -	A08-33, A10-8, A21-39, B11-40,
MD BIT 7	21 -	A08-35, A10-21, A21-41, B11-54,
MD BIT 8	21 -	A09-46, A21-43, B10-45, B12-43,
MD BIT 9	21 -	A09-44, A21-45, B10-52, B12-23,
MD BIT 10	21 -	A09-60, A21-47, B10-46, B12-58,
MD BIT 11	21 -	A09-43, A21-49, B10-55, B12-47,
MD BIT 12	21 -	A09-27, A21-51, B10-57, B12-56,
MD BIT 13	21 -	A09-39, A21-53, B10-54, B12-57,
MD BIT 14	21 -	A09-25, A21-55, B10-44, B12-22,
MD BIT 15	21 -	A09-38, A21-57, B10-56, B12-42,
MD BIT 16	21 -	A19-34, A21-59,
MD BIT 17	21 -	A21-61, B19-29,
MD BIT 0	21 -	A08-7, A10-19, A21-27, B11-41,
MD SUB	13 +	A13-26, A15-46,

SIGNAL		CONNECTIONS
MD SUB	13 -	A13-18,
MDM	17 +	A16-23, B17-8,
MDX	17 +	B16-50, B17-38,
MDX SKIP	13 +	A13-39, B16-12,
MEM READ	20 +	A20-62, A21-25,
MEM WRITE	20 +	A20-60, A21-24,
MPY	17 -	B13-38, B15-9, B17-2,
MPY E1	15 +	B13-8, B15-5, B16-47,
MPY E2	15 +	A13-25, A15-62,
MPY HOLD T7	17 -	A17-35, B12-27,
MPY SHIFT	13 +	B13-7,
MPY SHIFT	13 -	A15-41, A17-38, B12-28, B13-23,
MPY 0 RST CCC, EXT	13 -	A10-61, A13-45,
NO CONNECTION	8	A08-6, A08-8, A08-12, A08-14, A08-23, A08-31, A08-32,
NO CONNECTION	9	A09-5, A09-6, A09-8, A09-12, A09-13,
NO CONNECTION	10	A10-28, A10-34, A10-38, B10-20, B10-21, B10-22, B10-28, B10-30, B10-32, B10-36, B10-38, B10-39, B10-40, B10-42, B10-58,
NO CONNECTION	11	B11-33, B11-39,
NO CONNECTION	12	A12-17, B12-20, B12-38,
NO CONNECTION	14	B14-27, B14-29, B14-35, B14-38, B14-40, B14-47, B14-53, B14-55, B14-58,
NO CONNECTION	15	A15-14, A15-20, A15-22, A15-24, B15-28,
NO CONNECTION	16	A16-8, A16-14,
NO CONNECTION	18	B18-40, B18-54, B18-55, B18-56, B18-57, B18-58,

SIGNAL		CONNECTIONS
NO CONNECTION	20	A20-5, A20-6, A20-10, A20-30, B20-12, B20-14, B20-20, B20-28, B20-33, B20-39, B20-40, B20-44, B20-46, B20-47, B20-49, B20-54, B20-55, B20-56, B20-57, B20-58,
NO CONNECTION	21	A21-3, B21-3, B21-39, B21-50, B21-52, B21-54, B21-58, B21-59, B21-60,
NO CONNECTION	22	A22-57, A22-59, A22-61,
NO E CYCLE	17 +	B13-31, B17-47,
NO EA OP	17 -	A16-48, B13-16, B17-37,
NO LVL ACT	20 +	B14-43, B20-9,
OP BIT 0	11 -	A11-18, B16-21, B17-10,
OP BIT 1	11 -	A11-22, B17-23,
OP BIT 2	11 -	A11-23, B17-24,
OP BIT 3	11 -	A11-57, B17-35,
OP BIT 4	11 -	A11-45, A13-49, A15-36, B17-34,
OP BIT 5	11 -	A11-54, A13-47, B14-51, B17-42,
OP BIT 6	11 -	A11-41, B12-10, B15-32,
OP BIT 7	11 -	A11-43, B12-12, B15-36,
OP BIT 8	12 -	A11-7, A17-10, B12-14, B15-37,
OP BIT 9	12 -	A17-41, B12-3, B15-10, B16-29, B19-22,
OP BIT 10	12 -	A15-9, B12-19, B14-33,
OP BIT 11	12 -	A15-17, B12-17, B14-48,
OP BIT 12	12 -	B12-39, B15-26,
OP BIT 13	12 -	A15-16, B12-41, B13-26,
OP BIT 14	12 -	A13-31, A15-25, B12-21,
OP BIT 15	12 -	A15-19, B12-18, B19-7,
OP BIT 5	11 +	A11-27, B15-38, B16-56,

COMPUTER HARDWARE INC.

SIGNAL		CONNECTIONS
OP CHECK	19 +	A18-36, A19-31,
OP CHECK	19 -	A19-33, A22-6,
OR	17 -	A15-30, B17-6,
OVERFLOW	13 +	A13-43,
OVERFLOW	13 -	A15-34, B13-13,
OVERFLOW ENAB RST	15 +	A13-62, A15-57,
OVERFLOW ENAB SET	15 +	A13-59, B15-35,
PAR CHK	19 +	A18-53, A19-47,
PAR CHK	19 -	A19-49, B22-42,
PARITY 0-7 EVEN	11 +	A12-53, B11-34,
PES 4	22 -	A14-51, A22-35,
PES 5	22 -	A14-50, A22-37,
PES 6	22 -	A14-52, A22-39,
PES 7	22 -	A14-42, A22-41,
PHASE A REF	11 -	A11-60, A18-50, A19-32, B12-54, B20-26,
POLL	18 +	A18-41, B14-13,
POLL INT	18 +	B18-2, B20-3,
POWER SUPPLY CONN	8	A08-1, A08-2, A08-3, A08-4, B08-59, B08-60, B08-61, B08-62,
POWER SUPPLY CONN	9	A09-1, A09-2, A09-3, A09-4, B09-59, B09-60, B09-61, B09-62,
POWER SUPPLY CONN	10	A10-1, A10-2, A10-3, A10-4, B10-59, B10-60, B10-61, B10-62,
POWER SUPPLY CONN	11	A11-1, A11-2, A11-3, A11-4, B11-59, B11-60, B11-61, B11-62,
POWER SUPPLY CONN	12	A12-1, A12-2, A12-3, A12-4, B12-59, B12-60, B12-61, B12-62,
POWER SUPPLY CONN	13	A13-1, A13-2, A13-3, A13-4, B13-59,

SIGNAL		CONNECTIONS
POWER SUPPLY CONN	13	B13-60, B13-61, B13-62,
POWER SUPPLY CONN	14	A14-1, A14-2, A14-3, A14-4, B14-59, B14-60, B14-61, B14-62,
POWER SUPPLY CONN	15	A15-1, A15-2, A15-3, A15-4, B15-59, B15-60, B15-61, B15-62,
POWER SUPPLY CONN	16	A16-1, A16-2, A16-3, A16-4, B16-59, B16-60, B16-61, B16-62,
POWER SUPPLY CONN	17	A17-1, A17-2, A17-3, A17-4, B17-59, B17-60, B17-61, B17-62,
POWER SUPPLY CONN	18	A18-1, A18-2, A18-3, A18-4, B18-59, B18-60, B18-61, B18-62,
POWER SUPPLY CONN	19	A19-1, A19-2, A19-3, A19-4, B19-59, B19-60, B19-61, B19-62,
POWER SUPPLY CONN	20	A20-1, A20-2, A20-3, A20-4, B20-59, B20-60, B20-61, B20-62,
POWER SUPPLY CONN	21	A21-1, A21-2, B21-61, B21-62,
POWER SUPPLY CONN	22	A22-1, A22-2, A22-3, A22-4, B22-59, B22-60, B22-61, B22-62,
PROG CTL RST S-300	22 -	A19-40, B22-29,
PROG LOAD	19 +	A18-15, A19-57,
PROG LOAD S-311	22 -	A19-13, B22-21,
PROG STOP	19 -	B19-21, B20-16,
PWR ON RST	18 -	A18-24, B19-15,
QUOT CORR	13 +	A13-17, B15-16,
QUOT CORR	13 -	A13-19,
READ	18 -	A11-53, A14-40, B16-33, B17-48, B18-32,
READ+WRITE	18 +	A13-48, A16-61, B18-35,
RESET INT	17 -	A20-9, B17-36,
RESET OPR	15 -	A11-42, A15-35, B12-35,

SIGNAL		CONNECTIONS
RESET S-308	22 -	A22-14, B19-6,
RROP	17 +	A16-52, B13-27, B17-33,
RROP	17 -	A15-59, A16-25, B17-31,
RST ACC	16 -	A10-45, B16-58,
RST DRG	16 +	A10-47, B16-4,
RST EXTEND	18 +	B11-6, B18-41,
RST TAC	16 -	A10-7, B16-15,
RUN	12 -	A17-48, A19-48, B12-1,
RUN + SS MODE	12 -	B11-18, B12-6,
RUN LAMP	19 -	A19-6, A22-10,
RUN S-112	22 -	A17-49, B19-11, B22-17,
S CYCLE S-112	22 -	A12-9, A22-49, B11-37,
S INST S-112	22 -	B19-27, B22-9,
S STEP S-112	22 -	A22-45, B11-2,
SAR CMP S-112	22 -	A22-47, B17-58,
SBR BIT 0	8 +	A08-59, B11-25, B18-26, B20-10,
SBR BIT 1	8 +	A08-58, A18-56, B11-27, B20-7,
SBR BIT 2	8 +	A08-44, B11-28, B18-30,
SBR BIT 3	8 +	A08-56, A18-8, B11-30,
SBR BIT 4	8 +	A08-39, B11-32, B18-12,
SBR BIT 5	8 +	A08-54, A18-21, B11-29,
SBR BIT 6	8 +	A08-52, B11-5, B18-49,
SBR BIT 7	8 +	A08-47, A18-12, B11-3,
SBR BIT 8	9 +	A09-32, A12-47, B14-15, B18-43, B20-42,
SBR BIT 9	9 +	A09-58, A12-49, A14-43, A18-62, B20-53,

SIGNAL		CONNECTIONS
SBR BIT 10	9 +	A09-59, A12-50, A20-43, B14-12, B18-11,
SBR BIT 11	9 +	A09-48, A12-51, A18-33, A20-41,
SBR BIT 12	9 +	A09-47, A12-56, A20-32, B18-7,
SBR BIT 13	9 +	A09-19, A12-57, A18-16, A20-42,
SBR BIT 14	9 +	A09-53, A12-52, B18-5, B20-13,
SBR BIT 15	9 +	A09-50, A12-48, A18-47, B20-1,
SBR PARITY ODD	12 -	A12-55, B19-51,
SEL HEXD A	17 +	B08-20, B09-9, B17-51,
SEL HEXD B	17 +	A17-55, B08-26, B09-7,
SELECT CSM 1	8 +	A21-16, B08-19,
SELECT CSM 2	8 +	A21-17, B08-18,
SELECT CSM 3	8 +	A21-18, B08-40,
SELECT CSM 4	8 +	A21-19, B08-39,
SELECT CSM 5	8 +	A21-20, B08-42,
SELECT CSM 6	8 +	A21-21, B08-32,
SELECT CSM 7	8 +	A21-22, B08-44,
SELECT CSM 8	8 +	A21-23, B08-10,
SELECT DISPLAY 1	XX +	B22-20,
SENSE DEV	18 -	A14-62, B18-36, B20-17,
SENSE OP	18 -	A18-52, B16-27, B17-21,
SES 0	22 -	A14-13, A22-16,
SES 1	22 -	A14-18, A22-18,
SES 2	22 -	A14-32, A22-20,
SES 3	22 -	A14-7, A22-22,
SET BSI	15 -	B11-20, B12-24, B15-2,

SIGNAL		CONNECTIONS
SHOP SHIFT	13 +	A13-24, A15-38,
SHOP SHIFT	13 -	A13-55, A17-29, B11-48, B12-29,
SHOPS	17 +	A13-52, A16-24, B17-18,
SKIP COND	15 +	A15-40, B13-19, B16-38, B17-32,
SLC HOLD T7	13 +	A13-58,
SLC HOLD T7	13 -	A13-44, A16-6, A17-31, B11-43, B12-32,
SLCOP	17 +	B13-9, B17-57,
SP BIT	19 +	B11-47, B19-49,
SP BIT	19 -	B19-54,
SP CHECK	19 +	A18-9, A19-53,
SP CHECK	19 -	A19-55, B22-44,
SPARE	11	A11-48,
SPARE	12	A12-18,
SPARE	13	A13-36, B13-36,
SPARE	15	B15-54,
SPARE	16	A16-7, A16-10, A16-11, A16-34, A16-51, A16-59, B16-54,
SPARE	19	B19-42,
SPARE LAMP	XX -	A22-12,
SPARE S-307	22 -	B22-40,
SS MODE	11 +	B11-9,
SS MODE	11 -	A12-43, A17-43, A19-21, B11-10,
START CLOCK	19 +	A11-13, B19-35,
START REQ INT BSI	17 -	A17-44, B12-5, B14-56, B19-58,
START REQ P1	19 -	A19-54, B12-8,

SIGNAL		CONNECTIONS
START S-302	22 -	B19-2, B22-38,
START TCP STB	11 -	B11-12, B12-7, B19-20,
STD	17 -	A13-20, A17-57, B16-46,
STG ADD BIT 3	8 -	A21-62, B08-49,
STG ADD BIT 4	8 -	A21-4, B08-45,
STG ADD BIT 5	8 -	A21-5, B08-25,
STG ADD BIT 6	8 -	A21-6, B08-51,
STG ADD BIT 7	8 -	A21-7, B08-50,
STG ADD BIT 8	9 -	A21-8, B09-50,
STG ADD BIT 9	9 -	A21-9, B09-38,
STG ADD BIT 10	9 -	A21-10, B09-47,
STG ADD BIT 11	9 -	A21-11, B09-49,
STG ADD BIT 12	9 -	A21-12, B09-41,
STG ADD BIT 13	9 -	A21-13, B09-53,
STG ADD BIT 14	9 -	A21-14, B09-54,
STG ADD BIT 15	9 -	A21-15, B09-24,
STG PROT OPTION	XX +	A16-62,
STO	17 -	A13-5, A16-45, B17-7,
STOP	19 +	B19-18,
STOP S-301	22 -	B19-1, B22-36,
STOP T CLOCK	19 -	B12-2, B19-53,
STS	17 +	A15-51, B16-2, B17-49,
STSE	17 +	A13-51, A17-56, B19-41,
STX	17 -	B16-52, B17-5,
SUBOP	17 +	A17-61, B13-50, B15-20,

SIGNAL		CONNECTIONS
SYSCP REF P1	11 -	A17-53, B10-25, B11-52, B12-40, B13-18, B14-41,
SYSCP REF P2	11 -	A19-56, A20-59, B08-28, B09-43, B11-53, B15-49, B16-25,
SYSCP REF P3	12 -	A12-12,
T 0	12 -	A12-58, A18-54, A19-30, A20-56, B13-11, B16-45, B17-53,
T 1	12 -	A12-61, A16-31, A20-39, B15-52, B18-46, B19-57,
T 2	12 +	B12-26, B19-12,
T 2	12 -	A12-62, B15-50, B16-7, B17-41, B18-8,
T 3	12 -	A12-60, A16-53, A17-45, A19-37, A20-44, B13-14, B15-57, B18-45,
T 4	12 -	A12-46, A16-35, B13-4, B15-8, B18-4, B19-33,
T 5	12 -	A12-45, A13-50, A19-35, B15-39, B16-23, B17-54, B18-50,
T 6	12 +	A12-7, B11-22,
T 6	12 -	A12-8, A17-51, B13-3, B14-42, B15-25, B16-10, B18-24, B20-48,
T 7	12 -	A12-44, A17-20, B11-50, B13-2, B15-43, B16-35, B18-31,
TAC BIT 0	10 +	A10-22, A13-35, B15-29,
TAG	11 +	A11-5, A16-40, B13-12,
TAG	11 -	A11-6, B14-52, B17-44,
TAG X = 0	12 +	A16-12, B12-16,
TAG X = 7	12 +	A16-18, B12-15,
TAG Y = 0	12 -	A16-22, B12-13,
TAG Y = 7	12 -	A16-20, B12-33,
TCP RESET	11 -	A12-59, B11-11,

COMPUTER HARDWARE INC.

SIGNAL		CONNECTIONS
TEMP CARRY	13 +	A13-15, A15-11,
TRACE	19 +	B19-19, B20-18,
TRACE S-112	22 -	B14-31, B19-30, B22-11,
TO + XO RESET	19 -	A15-33, A19-39, B08-4, B09-58, B16-34,
WAIT	17 -	A12-13, A22-8, B17-12,
WRITE	18 -	A11-52, B17-30, B18-34,
WRT STG PRT S-110	22 -	A22-33, B19-8,
X 0	11 -	A11-55, A18-45, A19-50, A20-61, B15-3,
X 1	11 +	A11-40, B16-39, B18-42,
X 2	11 +	B11-17, B17-43, B18-25,
X 3	11 -	A11-58, A19-42, A20-58, B18-44,
X 4	11 +	A11-44, B18-29,
X 5	11 +	A11-46, A16-27, A19-38, B18-52,
X 6	11 +	A11-51, B18-27,
X 7	11 +	A16-44, B11-26, B18-37, B19-46,
XIO	17 -	A15-18, A17-13, A18-43, B11-38, B14-32, B16-13,
XO STB	19 -	A19-20,
ZERO REM	15 +	A13-13, B15-14, B16-51,

POINT LIST

POINT	SIGNAL		POINT	SIGNAL		POINT	SIGNAL	
A08-1	POWER SUPPLY CONN	8	A08-46	CLOCK SBR 0- 7	19 +	A09-29	BUS BIT 11	+
A08-2	POWER SUPPLY CONN	8	A08-47	SBR BIT 7	8 +	A09-30	IAR CARRY 8-15	9 +
A08-3	POWER SUPPLY CONN	8	A08-48	BUS BIT 6	+	A09-31	LAMP BUS 10	-
A08-4	POWER SUPPLY CONN	8	A08-49	CD BIT 7	8 -	A09-32	SBR BIT 8	9 +
A08-5	LAMP BUS 4	-	A08-50	CD BIT 0	8 -	A09-33	BUS BIT 9	+
A08-6	NO CONNECTION	8	A08-51	CD BIT 6	8 -	A09-34	LAMP BUS 15	-
A08-7	MD BIT 0	21 -	A08-52	SBR BIT 6	8 +	A09-35	LAMP BUS 11	-
A08-8	NO CONNECTION	8	A08-53	CD BIT 4	8 -	A09-36	BUS BIT 8	+
A08-9	GATE LAMPS P0	20 -	A08-54	SBR BIT 5	8 +	A09-37	ADV IAR GATE	16 +
A08-10	GATE LAMPS P2	20 -	A08-55	CD BIT 5	8 -	A09-38	MD BIT 15	21 -
A08-11	DC RESET	19 +	A08-56	SBR BIT 3	8 +	A09-39	MD BIT 13	21 -
A08-12	NO CONNECTION	8	A08-57	CD BIT 3	8 -	A09-40	LOAD IAR GATE	16 -
A08-13	MD BIT 2	21 -	A08-58	SBR BIT 1	8 +	A09-41	ENOP 3	XX -
A08-14	NO CONNECTION	8	A08-59	SBR BIT 0	8 +	A09-42	LAMP BUS 13	-
A08-15	GATE LAMPS P4	20 -	A08-60	GATE MD TO SBR	19 +	A09-43	MD BIT 11	21 -
A08-16	GATE LAMPS P1	20 -	A08-61	LAMP BUS 2	-	A09-44	MD BIT 9	21 -
A08-17	GATE STAT TO SBR	16 -	A08-62	LAMP BUS 3	-	A09-45	GATE MD TO SBR	19 +
A08-18	MD BIT 3	21 -	A09-1	POWER SUPPLY CONN	9	A09-46	MD BIT 8	21 -
A08-19	MD BIT 5	21 -	A09-2	POWER SUPPLY CONN	9	A09-47	SBR BIT 12	9 +
A08-20	BUS BIT 1	+	A09-3	POWER SUPPLY CONN	9	A09-48	SBR BIT 11	9 +
A08-21	LAMP BUS 7	-	A09-4	POWER SUPPLY CONN	9	A09-49	CD BIT 12	9 -
A08-22	BUS BIT 2	+	A09-5	NO CONNECTION	9	A09-50	SBR BIT 15	9 +
A08-23	NO CONNECTION	8	A09-6	NO CONNECTION	9	A09-51	CD BIT 15	9 -
A08-24	BUS BIT 0	+	A09-7	LAMP BUS 9	-	A09-52	CD BIT 10	9 -
A08-25	BUS BIT 5	+	A09-8	NO CONNECTION	9	A09-53	SBR BIT 14	9 +
A08-26	BUS BIT 3	+	A09-9	GATE LAMPS P0	20 -	A09-54	CD BIT 11	9 -
A08-27	BUS BIT 7	+	A09-10	DC RESET	19 +	A09-55	CD BIT 14	9 -
A08-28	BUS BIT 4	+	A09-11	GATE LAMPS P2	20 -	A09-56	CLOCK SBR 8-15	19 +
A08-29	MD BIT 4	21 -	A09-12	NO CONNECTION	9	A09-57	CD BIT 9	9 -
A08-30	MD BIT 1	21 -	A09-13	NO CONNECTION	9	A09-58	SBR BIT 9	9 +
A08-31	NO CONNECTION	8	A09-14	ADV IAR 0-7	9 +	A09-59	SBR BIT 10	9 +
A08-32	NO CONNECTION	8	A09-15	GATE LAMPS P4	20 -	A09-60	MD BIT 10	21 -
A08-33	MD BIT 6	21 -	A09-16	GATE LAMPS P1	20 -	A09-61	CD BIT 8	9 -
A08-34	LAMP BUS 0	-	A09-17	CD BIT 13	9 -	A09-62	MAR CMP	9 -
A08-35	MD BIT 7	21 -	A09-18	LAMP BUS 8	-	A10-1	POWER SUPPLY CONN	10
A08-36	LAMP BUS 1	-	A09-19	SBR BIT 13	9 +	A10-2	POWER SUPPLY CONN	10
A08-37	IAR CARRY 8-15	9 +	A09-20	BUS BIT 15	+	A10-3	POWER SUPPLY CONN	10
A08-38	LOAD IAR GATE	16 -	A09-21	BUS BIT 14	+	A10-4	POWER SUPPLY CONN	10
A08-39	SBR BIT 4	8 +	A09-22	LAMP BUS 12	-	A10-5	MD BIT 4	21 -
A08-40	LAMP BUS 5	-	A09-23	BUS BIT 13	+	A10-6	ALU MODE	15 +
A08-41	ADV IAR 0-7	9 +	A09-24	BUS BIT 12	+	A10-7	RST TAC	16 -
A08-42	LAMP BUS 6	-	A09-25	MD BIT 14	21 -	A10-8	MD BIT 6	21 -
A08-43	CD BIT 2	8 -	A09-26	BUS BIT 10	+	A10-9	MD BIT 1	21 -
A08-44	SBR BIT 2	8 +	A09-27	MD BIT 12	21 -	A10-10	ALU S2	15 +
A08-45	CD BIT 1	8 -	A09-28	LAMP BUS 14	-	A10-11	BUS BIT 6	+

DASN ----------

FILE NUMBER ----------

DRAWN I. DRAW

ORIGINATOR TOM WALTERS

CHECKED A. FREDELL

1ST/REV RLSE APPROVAL J. ROYER

1ST RLSED

REV RLSED 8-8-75

COMPUTER HARDWARE INC.

TYPE-SIZE SA

DWG. NO. 2342

REV. E

TITLE SIGNAL LIST 2131 CPU CAGE

SHEET 29 OF 42

POINT LIST

POINT	SIGNAL			POINT	SIGNAL			POINT	SIGNAL		
A10-12	BUS BIT 1		+	A10-57	LAMP BUS 5		-	A11-40	X 1	11	+
A10-13	BUS BIT 7		+	A10-58	EXT SO	15	+	A11-41	OP BIT 6	11	-
A10-14	MD BIT 3	21	-	A10-59	GATE ALU TO BUS	16	-	A11-42	RESET OPR	15	-
A10-15	ACC BIT 6	10	+	A10-60	ACC BIT 5	10	+	A11-43	OP BIT 7	11	-
A10-16	MD BIT 2	21	-	A10-61	MPY 0 RST CCC, EXT	13	-	A11-44	X 4	11	+
A10-17	ACC BIT 7	10	+	A10-62	ACC = 0	10	-	A11-45	OP BIT 4	11	-
A10-18	ALU S3	15	+	A11-1	POWER SUPPLY CONN	11		A11-46	X 5	11	+
A10-19	MD BIT 0	21	-	A11-2	POWER SUPPLY CONN	11		A11-47	GATE DISP TO TAC	16	-
A10-20	MD BIT 5	21	-	A11-3	POWER SUPPLY CONN	11		A11-48	SPARE	11	
A10-21	MD BIT 7	21	-	A11-4	POWER SUPPLY CONN	11		A11-49	GATE DISP TO DRG	16	-
A10-22	TAC BIT 0	10	+	A11-5	TAG	11	+	A11-50	E2 CYCLE	17	+
A10-23	GATE MD TO DRG 0- 7	16	-	A11-6	TAG	11	-	A11-51	X 6	11	+
A10-24	ALU S1	15	+	A11-7	OP BIT 8	12	-	A11-52	WRITE	18	-
A10-25	ACC BIT 2	10	+	A11-8	IXR ADD 2	15	+	A11-53	READ	18	-
A10-26	ALU BIT 0	10	+	A11-9	IXR ADD 1	15	+	A11-54	OP BIT 5	11	-
A10-27	ALU CN+4	10	-	A11-10	I/O IN BIT 7	14	+	A11-55	X 0	11	-
A10-28	NO CONNECTION	10		A11-11	I/O IN BIT 5	14	+	A11-56	LAMP BUS 7		-
A10-29	ACC BIT 0 SERIAL IN	15	+	A11-12	BUS BIT 7		+	A11-57	OP BIT 3	11	-
A10-30	BUS BIT 0		+	A11-13	START CLOCK	19	+	A11-58	X 3	11	-
A10-31	LAMP BUS 6		-	A11-14	BUS BIT 5		+	A11-59	GATE LAMPS P6	20	-
A10-32	BUS BIT 2		+	A11-15	I/O IN BIT 6	14	+	A11-60	PHASE A REF	11	-
A10-33	LAMP BUS 1		-	A11-16	I/O IN BIT 4	14	+	A11-61	GATE LAMPS P3	20	-
A10-34	NO CONNECTION	10		A11-17	BUS BIT 6		+	A11-62	GATE LAMPS P9-F	20	-
A10-35	LAMP BUS 7		-	A11-18	OP BIT 0	11	-	A12-1	POWER SUPPLY CONN	12	
A10-36	BUS BIT 3		+	A11-19	BUS BIT 4		+	A12-2	POWER SUPPLY CONN	12	
A10-37	ACC BIT 4	10	+	A11-20	LOAD IXR 0- 7 GATE	16	-	A12-3	POWER SUPPLY CONN	12	
A10-38	NO CONNECTION	10		A11-21	LAMP MPX A	20	+	A12-4	POWER SUPPLY CONN	12	
A10-39	ACC S1	15	+	A11-22	OP BIT 1	11	-	A12-5	IXR ADD 1	15	+
A10-40	LAMP BUS 2		-	A11-23	OP BIT 2	11	-	A12-6	LAMP MPX A	20	+
A10-41	ALU A=B	10	+	A11-24	IXR ADD 0	15	+	A12-7	T 6	12	+
A10-42	ACC SO	15	+	A11-25	LAMP MPX B	20	+	A12-8	T 6	12	-
A10-43	ACC BIT 3	10	+	A11-26	LAMP MPX C	20	+	A12-9	S CYCLE S-112	22	-
A10-44	ALU SO	15	+	A11-27	OP BIT 5	11	+	A12-10	GATE I/O TO SBR	17	-
A10-45	RST ACC	16	-	A11-28	GATE IXR TO BUS	16	-	A12-11	GATE I/O TO SBR + ACC	16	-
A10-46	DRG BIT 0	10	+	A11-29	I/O IN BIT 3	14	+	A12-12	SYSCP REF P5	12	-
A10-47	RST DRG	16	+	A11-30	I/O IN BIT 1	14	+	A12-13	WAIT	17	-
A10-48	ACC BIT 0	10	+	A11-31	BUS BIT 3		+	A12-14	GATE I/O TO DRG	17	-
A10-49	LAMP BUS 4		-	A11-32	LAMP BUS 4		-	A12-15	ERROR CHK	19	-
A10-50	LOAD DRG GATE	16	+	A11-33	BUS BIT 1		+	A12-16	GATE I/O TO BUS	12	-
A10-51	LAMP BUS 3		-	A11-34	I/O IN BIT 2	14	+	A12-17	NO CONNECTION	12	
A10-52	BUS BIT 5		+	A11-35	LAMP BUS 5		-	A12-18	SPARE	12	
A10-53	ACC BIT 1	10	+	A11-36	BUS BIT 2		+	A12-19	BUS BIT 15		+
A10-54	BUS BIT 4		+	A11-37	CS HOLD T7	11	-	A12-20	LAMP MPX B	20	+
A10-55	LAMP BUS 0		-	A11-38	BUS BIT 0		+	A12-21	BUS BIT 11		+
A10-56	EXT S1	15	+	A11-39	I/O IN BIT 0	14	+	A12-22	LAMP BUS 15		-

DASH: ----------

FILE NUMBER: ----------

DRAWN: I. DRAW

ORIGINATOR: TOM WALTERS

CHECKED: A. FREDELL

1ST/REV RLSE APPROVAL: J. ROYER

1ST RLSED

REV RLSED: 8-8-75

COMPUTER HARDWARE INC.

TYPE-SIZE: SA

DWG. NO.: 2342

REV.: E

TITLE: SIGNAL LIST 2131 CPU CAGE

POINT LIST

POINT	SIGNAL			POINT	SIGNAL			POINT	SIGNAL		
A12-23	BUS BIT 10		+	A13-6	EXT BIT 15	10	+	A13-51	STSE	17	+
A12-24	IXR ADD 2	15	+	A13-7	DRG BIT 0	10	+	A13-52	SHOPS	17	+
A12-25	LAMP BUS 10		-	A13-8	ALU SUB	15	+	A13-53	GATE CCC TO IXR	13	-
A12-26	LAMP BUS 9		-	A13-9	ALU CN+4	10	-	A13-54	DBL PREC OP	17	+
A12-27	IMM STOP	19	+	A13-10	ALU CARRY OUT	13	+	A13-55	SHOP SHIFT	13	-
A12-28	BUS BIT 8		+	A13-11	ACC BIT 0	10	+	A13-56	ALU A=B	10	+
A12-29	BUS BIT 9		+	A13-12	ACC BIT 0 = DRG BIT 0	13	-	A13-57	COMP EQUAL	13	-
A12-30	LAMP BUS 8		-	A13-13	ZERO REM	15	+	A13-58	SLC HOLD T7	13	+
A12-31	GATE LAMPS P7	20	-	A13-14	CARRY TO ALU	15	+	A13-59	OVERFLOW ENAB SET	15	+
A12-32	GATE LAMPS P9-F	20	-	A13-15	TEMP CARRY	13	+	A13-60	E CYCLES	17	-
A12-33	GATE LAMPS P6	20	-	A13-16	ALU CN	13	-	A13-61	COMP EQUAL	13	+
A12-34	LAMP BUS 11		-	A13-17	QUOT CORR	13	+	A13-62	OVERFLOW ENAB RST	15	+
A12-35	GATE LAMPS P3	20	-	A13-18	MD SUB	13	-	A14-1	POWER SUPPLY CONN	14	
A12-36	LAMP BUS 12		-	A13-19	QUOT CORR	13	-	A14-2	POWER SUPPLY CONN	14	
A12-37	ADV TCP	12	+	A13-20	STD	17	-	A14-3	POWER SUPPLY CONN	14	
A12-38	LAMP BUS 13		-	A13-21	INH ALU TO ACC	13	+	A14-4	POWER SUPPLY CONN	14	
A12-39	BUS BIT 13		+	A13-22	DIFF SIGN	13	-	A14-5	CES 10	XX	-
A12-40	LAMP BUS 14		-	A13-23	DIV E1	15	+	A14-6	DES 10	22	-
A12-41	LAMP MPX C	20	+	A13-24	SHOP SHIFT	13	+	A14-7	SES 3	22	-
A12-42	GATE IXR TO BUS	16	-	A13-25	MPY E2	15	+	A14-8	I/F IN BIT 8		-
A12-43	SS MODE	11	-	A13-26	MD SUB	13	+	A14-9	DES 3	22	-
A12-44	T 7	12	-	A13-27	E1 CYCLE	17	-	A14-10	I/F IN BIT 10		-
A12-45	T 5	12	-	A13-28	ALU BIT 0	10	+	A14-11	INT VEC BIT 0	20	-
A12-46	T 4	12	-	A13-29	ALU = 0	10	-	A14-12	DES 11	22	-
A12-47	SBR BIT 8	9	+	A13-30	CMPOP	17	+	A14-13	SES 0	22	-
A12-48	SBR BIT 15	9	+	A13-31	OP BIT 14	12	-	A14-14	DES 0	22	-
A12-49	SBR BIT 9	9	+	A13-32	GATE IXR TO CCC	13	-	A14-15	I/F IN BIT 0		-
A12-50	SBR BIT 10	9	+	A13-33	DIFF SIGN	13	+	A14-16	CES 8	XX	-
A12-51	SBR BIT 11	9	+	A13-34	EXT BIT 14	10	+	A14-17	I/F IN BIT 1		-
A12-52	SBR BIT 14	9	+	A13-35	TAC BIT 0	10	+	A14-18	SES 1	22	-
A12-53	PARITY 0-7 EVEN	11	+	A13-36	SPARE	13		A14-19	DES 1	22	-
A12-54	CD BIT 17	12	-	A13-37	COMP LESS OR EQUAL	13	+	A14-20	GATE DES TO I/O	19	-
A12-55	SBR PARITY ODD	12	-	A13-38	ACC BIT 1	10	+	A14-21	DES 2	22	-
A12-56	SBR BIT 12	9	+	A13-39	MDX SKIP	13	+	A14-22	CES 11	XX	-
A12-57	SBR BIT 13	9	+	A13-40	DRG = 0	10	-	A14-23	ENOP 4	XX	+
A12-58	T 0	12	-	A13-41	GATE SBR TO CCC	13	-	A14-24	I/F IN BIT 11		-
A12-59	TCP RESET	11	-	A13-42	LDS	17	+	A14-25	DES 8	22	-
A12-60	T 3	12	-	A13-43	OVERFLOW	13	+	A14-26	I/O IN BIT 8	14	+
A12-61	T 1	12	-	A13-44	SLC HOLD T7	13	-	A14-27	I/O IN BIT 9	14	+
A12-62	T 2	12	-	A13-45	MPY 0 RST CCC, EXT	13	-	A14-28	CES 9	XX	-
A13-1	POWER SUPPLY CONN	13		A13-46	LAST I	17	-	A14-29	I/O IN BIT 0	14	+
A13-2	POWER SUPPLY CONN	13		A13-47	OP BIT 5	11	-	A14-30	I/O IN BIT 11	14	+
A13-3	POWER SUPPLY CONN	13		A13-48	READ+WRITE	18	+	A14-31	I/O IN BIT 1	14	+
A13-4	POWER SUPPLY CONN	13		A13-49	OP BIT 4	11	-	A14-32	SES 2	22	-
A13-5	STO	17	-	A13-50	T 5	12	-	A14-33	I/O IN BIT 10	14	+

TYPE-SIZE: SA | DWG. NO.: 2342 | REV.: E | TITLE: SIGNAL LIST 2131 CPU CAGE | SHEET: 31 OF 42

DASH: ---------- | DRAWN: I. DRAW | CHECKED: A. FREDELL | 1ST RLSED | REV RLSED: 8-8-75

FILE NUMBER: ---------- | ORIGINATOR: TOM WALTERS | 1ST/REV RLSE APPROVAL: J. ROYER

COMPUTER HARDWARE INC.

POINT LIST

POINT	SIGNAL		POINT	SIGNAL		POINT	SIGNAL	
A14-34	I/O IN BIT 5	14 +	A15-17	OP BIT 11	12 -	A15-62	MPY E2	15 +
A14-35	I/O IN BIT 2	14 +	A15-18	XIO	17 -	A16-1	POWER SUPPLY CONN	16
A14-36	DES 9	22 -	A15-19	OP BIT 15	12 -	A16-2	POWER SUPPLY CONN	16
A14-37	I/O IN BIT 3	14 +	A15-20	NO CONNECTION	15	A16-3	POWER SUPPLY CONN	16
A14-38	I/F IN BIT 2	-	A15-21	IXR ADD 1	15 +	A16-4	POWER SUPPLY CONN	16
A14-39	I/F IN BIT 3	-	A15-22	NO CONNECTION	15	A16-5	DIOP	17 -
A14-40	READ	18 -	A15-23	GATE MD TO OPR	15 +	A16-6	SLC HOLD T7	13 -
A14-41	I/O IN BIT 7	14 +	A15-24	NO CONNECTION	15	A16-7	SPARE	16
A14-42	PES 7	22 -	A15-25	OP BIT 14	12 -	A16-8	NO CONNECTION	16
A14-43	SBR BIT 9	9 +	A15-26	GATE EXT TO ACC	16 -	A16-9	GATE DISP TO TAC	16 -
A14-44	DES 6	22 -	A15-27	GATE KDR TO ACC	19 +	A16-10	SPARE	16
A14-45	AREA 7	18 -	A15-28	CCC = 1	13 -	A16-11	SPARE	16
A14-46	DES 5	22 -	A15-29	GATE I/O TO SBR + ACC	16 -	A16-12	TAG X = 0	12 +
A14-47	I/F IN BIT 9	-	A15-30	OR	17 -	A16-13	GATE I/O TO DRG	17 -
A14-48	INT VEC BIT 15	20 -	A15-31	GATE ALU TO ACC	16 -	A16-14	NO CONNECTION	16
A14-49	DES 7	22 -	A15-32	BSC	17 -	A16-15	GATE IXR TO CCC	13 -
A14-50	PES 5	22 -	A15-33	TO + XO RESET	19 -	A16-16	GATE DISP TO DRG	16 -
A14-51	PES 4	22 -	A15-34	OVERFLOW	13 -	A16-17	LOAD DRG GATE	16 +
A14-52	PES 6	22 -	A15-35	RESET OPR	15 -	A16-18	TAG X = 7	12 +
A14-53	DES 4	22 -	A15-36	OP BIT 4	11 -	A16-19	GATE IXR TO OPR	15 -
A14-54	INT VEC BIT 12	20 -	A15-37	CARRY TO ALU	15 +	A16-20	TAG Y = 7	12 -
A14-55	I/F IN BIT 4	-	A15-38	SHOP SHIFT	13 +	A16-21	LOAD TAC GATE	16 +
A14-56	CES 12	XX -	A15-39	ACC S0	15 +	A16-22	TAG Y = 0	12 -
A14-57	I/F IN BIT 7	-	A15-40	SKIP COND	15 +	A16-23	MDM	17 +
A14-58	I/F IN BIT 5	-	A15-41	MPY SHIFT	13 -	A16-24	SHOPS	17 +
A14-59	I/O IN BIT 12	14 +	A15-42	I1 CYCLE	17 -	A16-25	RROP	17 -
A14-60	I/O IN BIT 15	14 +	A15-43	AND	17 -	A16-26	GATE I/O TO SBR + ACC	16 -
A14-61	INT ACK	17 -	A15-44	CMPOP	17 +	A16-27	X 5	11 +
A14-62	SENSE DEV	16 -	A15-45	ALU S3	15 +	A16-28	INDST	17 -
A15-1	POWER SUPPLY CONN	15	A15-46	MD SUB	13 +	A16-29	GATE ACC TO BUS	16 -
A15-2	POWER SUPPLY CONN	15	A15-47	LDS	17 +	A16-30	GATE MD TO DRG 0- 7	16 -
A15-3	POWER SUPPLY CONN	15	A15-48	E CYCLES	17 -	A16-31	T 1	12 -
A15-4	POWER SUPPLY CONN	15	A15-49	ACC = 0	10 -	A16-32	GATE KDR TO SBR	19 -
A15-5	CS LEVEL	11 -	A15-50	ALU MODE	15 +	A16-33	CCC = 0	13 -
A15-6	EXT BIT 0	10 +	A15-51	STS	17 +	A16-34	SPARE	16
A15-7	ALU S2	15 +	A15-52	INT BSI I1 I2	17 +	A16-35	T 4	12 -
A15-8	E2 CYCLE	17 +	A15-53	ACC S1	15 +	A16-36	DIV E	15 +
A15-9	OP BIT 10	12 -	A15-54	EXT S0	15 +	A16-37	GATE STAT TO SBR	16 -
A15-10	DBL PREC OP	17 +	A15-55	EXT S1	15 +	A16-38	EMCSL 123	9 -
A15-11	TEMP CARRY	13 +	A15-56	ALU S1	15 +	A16-39	GATE I/O TO SBR	17 -
A15-12	ADDOP	17 +	A15-57	OVERFLOW ENAB RST	15 +	A16-40	TAG	11 +
A15-13	ALU S0	15 +	A15-58	ACC BIT 0 SERIAL IN	15 +	A16-41	LOAD SBR GATE	16 +
A15-14	NO CONNECTION	15	A15-59	RROP	17 -	A16-42	IA CYCLE	17 -
A15-15	ACC BIT 15	10 +	A15-60	CARRY	13 -	A16-43	LDX	17 -
A15-16	OP BIT 13	12 -	A15-61	LAST I	17 -	A16-44	X 7	11 +

DASH ---

FILE NUMBER ----------

DRAWN I. DRAW

ORIGINATOR TOM WALTERS

CHECKED A. FREDELL

1ST/REV RLSE APPROVAL J. ROYER

1ST RLSED

REV RLSED 8-8-75

COMPUTER HARDWARE INC.

TYPE-SIZE SA

DWG. NO. 2342

REV. E

TITLE SIGNAL LIST 2131 CPU CAGE

SHEET 32 OF 42

POINT LIST

POINT	SIGNAL		POINT	SIGNAL		POINT	SIGNAL	
A16-45	STU	17 -	A17-28	CMP CHK IND	17 -	A18-11	I/F STG PRT ERR	18 -
A16-46	II CYCLE	17 -	A17-29	SHOP SHIFT	13 -	A18-12	SBR BIT 7	8 +
A16-47	CS LEVEL	11 -	A17-30	E2 CYCLE	17 +	A18-13	INH CS REQ	XX -
A16-48	NO EA OP	17 -	A17-31	SLC HOLD T7	13 -	A18-14	I/F OUT BIT 7	18 -
A16-49	GATE EXT TO ACC	16 -	A17-32	KEY ACTIVE	19 +	A18-15	PROG LOAD	19 +
A16-50	E2 CYCLE	17 +	A17-33	DIV CMP HOLD T7	13 -	A18-16	SBR BIT 13	9 +
A16-51	SPARE	16	A17-34	CCC = 1	13 -	A18-17	I/F PROG LOAD	18 -
A16-52	RROP	17 +	A17-35	MPY HOLD T7	17 -	A18-18	I/F OUT BIT 13	18 -
A16-53	T 3	12 -	A17-36	E CYCLES	17 -	A18-19	I/F INH CS REQ	18 +
A16-54	GATE MAR TO BUS	16 -	A17-37	INT BSI I1 I2	17 +	A18-20	I/F OUT BIT 5	18 -
A16-55	GATE IXR TO BUS	16 -	A17-38	MPY SHIFT	13 -	A18-21	SBR BIT 5	8 +
A16-56	ADV TCP	12 +	A17-39	INT REQ	20 -	A18-22	I/F PROG LOAD BUSY	21 -
A16-57	LOAD MAR STB	16 -	A17-40	LAST I	17 -	A18-23	I/F RESET EXTEND	21 -
A16-58	GATE SBR TO IXR P2	16 -	A17-41	OP BIT 9	12 -	A18-24	PWR ON RST	18 -
A16-59	SPARE	16	A17-42	ADV TCP	12 +	A18-25	END OP	17 +
A16-60	GATE CCC TO IXR	13 -	A17-43	SS MODE	11 -	A18-26	I/F BLOCK CLOCK	21 -
A16-61	READ+WRITE	18 +	A17-44	START REQ INT BSI	17 -	A18-27	CPU CLOCK	17 -
A16-62	STG PROT OPTION	XX +	A17-45	T 5	12 -	A18-28	I/F IN BIT 2	-
A17-1	POWER SUPPLY CONN	17	A17-46	INH INTERRUPT	14 +	A18-29	I/F IN BIT 0	-
A17-2	POWER SUPPLY CONN	17	A17-47	DBL PREC OP	17 +	A18-30	GATE ILSW	18 +
A17-3	POWER SUPPLY CONN	17	A17-48	RUN	12 -	A18-31	I/F CPU CLOCK	18 +
A17-4	POWER SUPPLY CONN	17	A17-49	RUN S-112	22 -	A18-32	I/F FUNC CLEAR	18 -
A17-5	BSI	17 -	A17-50	COND RUN	17 +	A18-33	SBR BIT 11	9 +
A17-6	CMP CHK	17 -	A17-51	T 6	12 -	A18-34	CS LEVEL	11 +
A17-7	END OP	17 +	A17-52	GATE INT	17 +	A18-35	I/F OUT BIT 11	18 -
A17-8	IA CYCLE	17 -	A17-53	SYSCP REF P1	11 -	A18-36	OP CHECK	19 +
A17-9	INH STOR	17 -	A17-54	GATE I/O TO DRG	17 -	A18-37	I/F CS REQ	21 -
A17-10	OP BIT 8	12 -	A17-55	SEL HEXD B	17 +	A18-38	I/F OUT BIT 15	18 -
A17-11	LAMP BUS 4	-	A17-56	STSE	17 +	A18-39	I/F IN BIT 1	-
A17-12	E1 CYCLE	17 -	A17-57	STD	17 -	A18-40	I/F CS CYCLE	18 -
A17-13	XIO	17 -	A17-58	BSIE	17 +	A18-41	POLL	18 +
A17-14	LAMP BUS 2	-	A17-59	ADDOP	17 +	A18-42	INT REQ A	-
A17-15	II CYCLE	17 -	A17-60	LDOP	17 +	A18-43	XIO	17 -
A17-16	LAMP BUS 5	-	A17-61	SUBOP	17 +	A18-44	ACT LVL A	20 -
A17-17	LAMP BUS 0	-	A17-62	CMPOP	17 +	A18-45	X 0	11 -
A17-18	LAMP BUS 1	-	A18-1	POWER SUPPLY CONN	18	A18-46	INT VEC BIT 15	20 +
A17-19	LAMP BUS 3	-	A18-2	POWER SUPPLY CONN	18	A18-47	SBR BIT 15	9 +
A17-20	T 7	12 -	A18-3	POWER SUPPLY CONN	18	A18-48	I/F PHASE A	18 -
A17-21	I1 CYCLE	17 -	A18-4	POWER SUPPLY CONN	18	A18-49	INT VEC BIT 13	20 +
A17-22	LDX OP BIT 10	14 -	A18-5	I/F CS DATA STORE	21 -	A18-50	PHASE A REF	11 -
A17-23	I2 CYCLE	17 -	A18-6	I/F PWR ON RST	18 -	A18-51	I/F E2+E3	18 +
A17-24	DC RESET	19 +	A18-7	I/F OUT BIT 5	18 -	A18-52	SENSE OP	18 -
A17-25	CONSOLE S-112	22 -	A18-8	SBR BIT 3	8 +	A18-53	PAR CHK	19 +
A17-26	ADV CS CLOCK	11 +	A18-9	SP CHECK	19 +	A18-54	T 0	12 -
A17-27	GEN ADD BIT 15	17 +	A18-10	CHECK STOP S-111	22 -	A18-55	I/F PARITY ERR	18 -

DASH

FILE NUMBER ----------

DRAWN I. DRAW

ORIGINATOR TOM WALTERS

CHECKED A. FREDELL

1ST/REV RLSE APPROVAL J. ROYER

1ST RLSED

REV RLSED 8-8-75

COMPUTER HARDWARE INC.

TYPE-SIZE SA

DWG. NO. 2342

REV. E

TITLE SIGNAL LIST 2131 CPU CAGE

POINT LIST

POINT	SIGNAL		POINT	SIGNAL		POINT	SIGNAL	
A18-56	SBR BIT 1	8 +	A19-39	TO + XO RESET	19 -	A20-21	GATE LAMPS P4	20 -
A18-57	I/F OUT BIT 1	18 -	A19-40	PROG CTL RST S-300	22 -	A20-22	GATE LAMPS P5	20 -
A18-58	I/F E1+E3	18 +	A19-41	ENOP 1	XX +	A20-23	ACT LVL B	20 -
A18-59	INT VEC BIT 12	20 +	A19-42	X 3	11 -	A20-24	GATE LAMPS P6	20 -
A18-60	INT VEC BIT 14	20 +	A19-43	GATE KDR TO BUS	19 -	A20-25	GATE LAMPS P7	20 -
A18-61	I/F OUT BIT 9	18 -	A19-44	KEY DATA CLOCK	19 +	A20-26	ENAB LAMP MPX	XX -
A18-62	SBR BIT 9	9 +	A19-45	CLEAR STG S-304	22 -	A20-27	GATE LAMPS P8	20 -
A19-1	POWER SUPPLY CONN	19	A19-46	I/F PROG LOAD BUSY	21 -	A20-28	ACT LVL 3	20 -
A19-2	POWER SUPPLY CONN	19	A19-47	PAR CHK	19 +	A20-29	ACT LVL 0	20 -
A19-3	POWER SUPPLY CONN	19	A19-48	RUN	12 -	A20-30	NO CONNECTION	20
A19-4	POWER SUPPLY CONN	19	A19-49	PAR CHK	19 -	A20-31	LAMP MPX A	20 +
A19-5	GATE MD TO SBR	19 +	A19-50	X 0	11 -	A20-32	SBR BIT 12	9 +
A19-6	RUN LAMP	19 -	A19-51	KEY ACTIVE	19 +	A20-33	ACT LVL 1	20 -
A19-7	KEY 4	22 -	A19-52	KEY REG DATA	19 +	A20-34	LAMP MPX C	20 +
A19-8	KEY 3	22 -	A19-53	SP CHECK	19 +	A20-35	ACT LVL 4	20 -
A19-9	LOAD STG S-306	22 -	A19-54	START REQ P1	19 -	A20-36	LAMP MPX D	20 +
A19-10	LOAD ACC S-309	22 -	A19-55	SP CHECK	19 -	A20-37	GATE LAMPS P9-F	20 -
A19-11	KEY 6	22 -	A19-56	SYSCP REF P2	11 -	A20-38	EMCSL 123	9 -
A19-12	DISP STG S-303	22 -	A19-57	PROG LOAD	19 +	A20-39	T 1	12 -
A19-13	PROG LOAD S-311	22 -	A19-58	LOAD IAR S-300	22 -	A20-40	INT REQ	20 -
A19-14	KEY 5	22 -	A19-59	KEY 8	22 -	A20-41	SBR BIT 11	9 +
A19-15	CONS INT S-310	22 -	A19-60	KEY B	22 -	A20-42	SBR BIT 13	9 +
A19-16	CONSOLE S-112	22 -	A19-61	KEY D	22 -	A20-43	SBR BIT 10	9 +
A19-17	KEY 7	22 -	A19-62	KEY C	22 -	A20-44	T 3	12 -
A19-18	KEY 2	22 -	A20-1	POWER SUPPLY CONN	20	A20-45	INT VEC BIT 15	20 -
A19-19	KEY 0	22 -	A20-2	POWER SUPPLY CONN	20	A20-46	GATE ILSW	18 +
A19-20	XO STB	19 -	A20-2	ENAB LAMP MPX	XX -	A20-47	ACT LVL 5	20 -
A19-21	SS MODE	11 -	A20-3	POWER SUPPLY CONN	20	A20-48	INT VEC BIT 14	20 +
A19-22	KEY 1	22 -	A20-4	POWER SUPPLY CONN	20	A20-49	INT VEC BIT 15	20 +
A19-23	KEY A	22 -	A20-5	NO CONNECTION	20	A20-50	LAMP BUS 13	-
A19-24	CLEAR BUS T7	19 -	A20-6	NO CONNECTION	20	A20-51	LAMP BUS 11	-
A19-25	GATE KDR TO ACC	19 +	A20-7	GATE INT	17 +	A20-52	ACT LVL 2	20 -
A19-26	DC RESET P2	19 -	A20-8	DC RESET P2	19 -	A20-53	INH STOR	17 -
A19-27	GATE KDR TO IAR	19 -	A20-9	RESET INT	17 -	A20-54	INT VEC BIT 14	20 -
A19-28	KEY 9	22 -	A20-10	NO CONNECTION	20	A20-55	LAMP BUS 12	-
A19-29	CONSOLE INT	19 -	A20-11	LAMP BUS 15	-	A20-56	T 0	12 -
A19-30	T 0	12 -	A20-12	LAMP BUS 9	-	A20-57	LAMP BUS 10	-
A19-31	OP CHECK	19 +	A20-13	ACT LVL A	20 -	A20-58	X 3	11 -
A19-32	PHASE A REF	11 -	A20-14	GATE LAMPS PO	20 -	A20-59	SYSCP REF P2	11 -
A19-33	OP CHECK	19 -	A20-15	LAMP BUS 8	-	A20-60	MEM WRITE	20 +
A19-34	MD BIT 16	21 -	A20-16	GATE LAMPS P1	20 -	A20-61	X 0	11 -
A19-35	T 5	12 -	A20-17	GATE LAMPS P2	20 -	A20-62	MEM READ	20 +
A19-36	CLEAR MODE	19 -	A20-18	LAMP MPX B	20 +	A21-1	POWER SUPPLY CONN	21
A19-37	T 3	12 -	A20-19	GATE LAMPS P3	20 -	A21-2	POWER SUPPLY CONN	21
A19-38	X 5	11 +	A20-20	LAMP BUS 14	-	A21-3	NO CONNECTION	21

DASH: ----------

FILE NUMBER: ----------

DRAWN: I. DRAW

ORIGINATOR: TOM WALTERS

CHECKED: A. FREDELL

1ST/REV RLSE APPROVAL: J. ROYER

1ST RLSED:

REV RLSED: 8-8-75

TYPE/SIZE: SA

DWG. NO.: 2342

REV.: E

TITLE: SIGNAL LIST 2131 CPU CAGE

SHEET: 34 of 42

COMPUTER HARDWARE INC.

POINT LIST

POINT	SIGNAL		POINT	SIGNAL		POINT	SIGNAL	
A21-4	STG ADD BIT 4	8 -	A21-49	MD BIT 11	21 -	A22-32	DES 5	22 -
A21-5	STG ADD BIT 5	8 -	A21-50	CD BIT 12	9 -	A22-33	WRT STG PRT S-110	22 -
A21-6	STG ADD BIT 6	8 -	A21-51	MD BIT 12	21 -	A22-34	DES 6	22 -
A21-7	STG ADD BIT 7	8 -	A21-52	CD BIT 13	9 -	A22-35	PES 4	22 -
A21-8	STG ADD BIT 8	9 -	A21-53	MD BIT 13	21 -	A22-36	DES 7	22 -
A21-9	STG ADD BIT 9	9 -	A21-54	CD BIT 14	9 -	A22-37	PES 5	22 -
A21-10	STG ADD BIT 10	9 -	A21-55	MD BIT 14	21 -	A22-38	DES 8	22 -
A21-11	STG ADD BIT 11	9 -	A21-56	CD BIT 15	9 -	A22-39	PES 6	22 -
A21-12	STG ADD BIT 12	9 -	A21-57	MD BIT 15	21 -	A22-40	DES 9	22 -
A21-13	STG ADD BIT 13	9 -	A21-58	CD BIT 16	11 -	A22-41	PES 7	22 -
A21-14	STG ADD BIT 14	9 -	A21-59	MD BIT 16	21 -	A22-42	DES 10	22 -
A21-15	STG ADD BIT 15	9 -	A21-60	CD BIT 17	12 -	A22-43	CHECK STOP S-111	22 -
A21-16	SELECT CSM 1	8 +	A21-61	MD BIT 17	21 -	A22-44	DES 11	22 -
A21-17	SELECT CSM 2	8 +	A21-62	STG ADD BIT 3	8 -	A22-45	S STEP S-112	22 -
A21-18	SELECT CSM 3	8 +	A22-1	POWER SUPPLY CONN	22	A22-46	LAMP BUS 5	-
A21-19	SELECT CSM 4	8 +	A22-2	POWER SUPPLY CONN	22	A22-47	SAR CMP S-112	22 -
A21-20	SELECT CSM 5	8 +	A22-3	POWER SUPPLY CONN	22	A22-48	LAMP BUS 1	-
A21-21	SELECT CSM 6	8 +	A22-4	POWER SUPPLY CONN	22	A22-49	S CYCLE S-112	22 -
A21-22	SELECT CSM 7	8 +	A22-5	HEX BIT 0	8 +	A22-50	LAMP BUS 16	-
A21-23	SELECT CSM 8	8 +	A22-6	OP CHECK	19 -	A22-51	DISP/SP S-112	22 -
A21-24	MEM WRITE	20 +	A22-7	HEX BIT 2	8 +	A22-52	LAMP BUS 15	-
A21-25	MEM READ	20 +	A22-8	WAIT	17 -	A22-53	LAMP BUS 0	-
A21-26	CD BIT 0	8 -	A22-9	HEX BIT 7	8 +	A22-54	LAMP BUS 3	-
A21-27	MD BIT 0	21 -	A22-10	RUN LAMP	19 -	A22-55	LAMP BUS 2	-
A21-28	CD BIT 1	8 -	A22-11	HEX BIT 15	9 +	A22-56	LAMP BUS 4	-
A21-29	MD BIT 1	21 -	A22-12	SPARE LAMP	XX -	A22-57	NO CONNECTION	22
A21-30	CD BIT 2	8 -	A22-13	HEX BIT 11	9 +	A22-58	LAMP BUS 8	-
A21-31	MD BIT 2	21 -	A22-14	RESET S-308	22 -	A22-59	NO CONNECTION	22
A21-32	CD BIT 3	8 -	A22-15	HEX BIT 3	8 +	A22-60	LAMP BUS 17	-
A21-33	MD BIT 3	21 -	A22-16	SES 0	22 -	A22-61	NO CONNECTION	22
A21-34	CD BIT 4	8 -	A22-17	HEX BIT 1	8 +	A22-62	LAMP BUS 7	-
A21-35	MD BIT 4	21 -	A22-18	SES 1	22 -	B03-1	ACC BIT 0	10 +
A21-36	CD BIT 5	8 -	A22-19	HEXD ENAB	17 -	B03-2	HEX BIT 0	8 +
A21-37	MD BIT 5	21 -	A22-20	SES 2	22 -	B08-3	ACC BIT 1	10 +
A21-38	CD BIT 6	8 -	A22-21	HEX BIT 5	8 +	B08-4	TO + XO RESET	19 -
A21-39	MD BIT 6	21 -	A22-22	SES 3	22 -	B08-5	HEX BIT 2	8 +
A21-40	CD BIT 7	8 -	A22-23	HEX BIT 10	9 +	B08-6	ACC BIT 2	10 +
A21-41	MD BIT 7	21 -	A22-24	INT DISABLE S-109	22 -	B08-7	HEX BIT 3	8 +
A21-42	CD BIT 8	9 -	A22-25	HEX BIT 8	9 +	B08-8	ACC BIT 3	10 +
A21-43	MD BIT 8	21 -	A22-26	DES 2	22 -	B08-9	MAR CMP P1	8 +
A21-44	CD BIT 9	9 -	A22-27	HEX BIT 13	9 +	B08-10	SELECT CSM 8	8 +
A21-45	MD BIT 9	21 -	A22-28	DES 3	22 -	B08-11	LOAD MAR STB	16 -
A21-46	CD BIT 10	9 -	A22-29	KEY 0	22 -	B08-12	ENAB IXR P1	8 +
A21-47	MD BIT 10	21 -	A22-30	DES 4	22 -	B08-13	ACC BIT 6	10 +
A21-48	CD BIT 11	9 -	A22-31	KEY 1	22 -	B08-14	DSR CLOCK	XX +

TYPE-SIZE: SA | DWG. NO.: 2342 | REV.: E | TITLE: SIGNAL LIST 2131 CPU CAGE | SHEET: 35 OF 42

DASH: ---------- | FILE NUMBER: ----------

DRAWN: I. DRAW | CHECKED: A. FREDELL | 1ST RLSED

ORIGINATOR: TOM WALTERS | 1ST/REV RLSE APPROVAL: J. ROYER | REV RLSED: 8-8-75

COMPUTER HARDWARE INC.

POINT LIST

POINT	SIGNAL		POINT	SIGNAL		POINT	SIGNAL	
B08-15	HEX BIT 6	8 +	B08-60	POWER SUPPLY CONN	8	B09-43	SYSCP REF P2	11 -
B08-16	ACC BIT 7	10 +	B08-61	POWER SUPPLY CONN	8	B09-44	GATE DSR TO BUS	XX -
B08-17	HEX BIT 7	8 +	B08-62	POWER SUPPLY CONN	8	B09-45	I/O IN BIT 10	14 +
B08-18	SELECT CSM 2	8 +	B09-1	ACC BIT 14	10 +	B09-46	HOLD CS ADD (X7)	11 +
B08-19	SELECT CSM 1	8 +	B09-2	HEX BIT 10	9 +	B09-47	STG ADD BIT 10	9 -
B08-20	SEL HEXD A	17 +	B09-3	ACC BIT 10	10 +	B09-48	I/O IN BIT 11	14 +
B08-21	I/O IN BIT 7	14 +	B09-4	HEX BIT 11	9 +	B09-49	STG ADD BIT 11	9 -
B08-22	ENAB SAR BIT 0	14 +	B09-5	ACC BIT 11	10 +	B09-50	STG ADD BIT 8	9 -
B08-23	GATE DSR TO BUS	XX -	B09-6	HEX BIT 14	9 +	B09-51	GATE SBR TO BUS	15 -
B08-24	HEX BIT 1	8 +	B09-7	SEL HEXD B	17 +	B09-52	I/O IN BIT 9	14 +
B08-25	STG ADD BIT 5	8 -	B09-8	HEX BIT 15	9 +	B09-53	STG ADD BIT 13	9 -
B08-26	SEL HEXD B	17 +	B09-9	SEL HEXD A	17 +	B09-54	STG ADD BIT 14	9 -
B08-27	GATE MAR TO BUS	16 -	B09-10	KEY DATA 8	9 +	B09-55	I/O IN BIT 8	14 +
B08-28	SYSCP REF P2	11 -	B09-11	HEX BIT 8	9 +	B09-56	GATE IAR TO BUS	16 -
B08-29	GATE KDR TO BUS	19 -	B09-12	ACC BIT 15	10 +	B09-57	GATE MAR TO BUS	16 -
B08-30	GATE SBR TO BUS	15 -	B09-13	ACC BIT 12	10 +	B09-58	TO + XO RESET	19 -
B08-31	ACC BIT 4	10 +	B09-14	ACC BIT 9	10 +	B09-59	POWER SUPPLY CONN	9
B08-32	SELECT CSM 6	8 +	B09-15	HEX BIT 12	9 +	B09-60	POWER SUPPLY CONN	9
B08-33	HEX BIT 4	8 +	B09-16	ACC BIT 13	10 +	B09-61	POWER SUPPLY CONN	9
B08-34	I/O IN BIT 6	14 +	B09-17	HEX BIT 13	9 +	B09-62	POWER SUPPLY CONN	9
B08-35	HEX BIT 5	8 +	B09-18	HEX BIT 9	9 +	B10-1	EXT BIT 0	10 +
B08-36	ACC BIT 5	10 +	B09-19	ACC BIT 8	10 +	B10-2	ACC BIT 15 SERIAL IN	15 +
B08-37	I/O IN BIT 5	14 +	B09-20	LOAD MAR STB	16 -	B10-3	BUS BIT 13	+
B08-38	I/O IN BIT 4	14 +	B09-21	KEY REG DATA	19 +	B10-4	BUS BIT 12	+
B08-39	SELECT CSM 4	8 +	B09-22	MAR CMP P1	8 +	B10-5	BUS BIT 15	+
B08-40	SELECT CSM 3	8 +	B09-23	KEY DATA CLOCK	19 +	B10-6	ACC BIT 14	10 +
B08-41	ADV CS CLOCK	11 +	B09-24	STG ADD BIT 15	9 -	B10-7	ACC BIT 6	10 +
B08-42	SELECT CSM 5	8 +	B09-25	MAR 4-7 = 0	8 +	B10-8	BUS BIT 14	+
B08-43	I/O IN BIT 2	14 +	B09-26	I/O IN BIT 15	14 +	B10-9	ACC BIT 9	10 +
B08-44	SELECT CSM 7	8 +	B09-27	INH STOR	17 -	B10-10	ALU = 0	10 -
B08-45	STG ADD BIT 4	8 -	B09-28	I/O IN BIT 14	14 +	B10-11	ACC BIT 10	10 +
B08-46	I/O IN BIT 3	14 +	B09-29	ENAB IXR P1	8 +	B10-12	BUS BIT 10	+
B08-47	GATE IAR TO BUS	16 -	B09-30	MAR CMP P2	8 +	B10-13	ACC BIT 11	10 +
B08-48	KEY DATA 8	9 +	B09-31	ENAB IXR P2	8 +	B10-14	GATE ACC TO BUS	16 -
B08-49	STG ADD BIT 3	8 -	B09-32	I/O IN BIT 13	14 +	B10-15	ALU CN	13 -
B08-50	STG ADD BIT 7	8 -	B09-33	MAR BIT 14	9 +	B10-16	BUS BIT 8	+
B08-51	STG ADD BIT 6	8 -	B09-34	MAR BIT 15	9 +	B10-17	DRG = 0	10 -
B08-52	MAR 4-7 = 0	8 +	B09-35	EMCSL 123	9 -	B10-18	BUS BIT 11	+
B08-53	ENAB IXR P2	8 +	B09-36	DSR CLOCK	XX +	B10-19	GATE EXT TO BUS	16 -
B08-54	I/O IN BIT 0	14 +	B09-37	I/O IN BIT 12	14 +	B10-20	NO CONNECTION	10
B08-55	MAR CMP P2	8 +	B09-38	STG ADD BIT 9	9 -	B10-21	NO CONNECTION	10
B08-56	KEY DATA CLOCK	19 +	B09-39	GEN ADD BIT 15	17 +	B10-22	NO CONNECTION	10
B08-57	I/O IN BIT 1	14 +	B09-40	ADV CS CLOCK	11 +	B10-23	ACC BIT 12	10 +
B08-58	HOLD CS ADD (X7)	11 +	B09-41	STG ADD BIT 12	9 -	B10-24	BUS BIT 9	+
B08-59	POWER SUPPLY CONN	8	B09-42	GATE KDR TO BUS	19 -	B10-25	SYSCP REF P1	11 -

DASIN

FILE NUMBER

DRAWN I. DRAW

ORIGINATOR TOM WALTERS

CHECKED A. FREDELL

1ST/REV RLSE APPROVAL J. ROYER

1ST RLSED

REV RLSED 8-8-75

TYPE-SIZE SA

DWG. NO. 2342

REV. E

TITLE SIGNAL LIST 2131 CPU CAGE

SHEET 36 OF 42

COMPUTER HARDWARE INC.

POINT LIST

POINT	SIGNAL			POINT	SIGNAL			POINT	SIGNAL		
P10-26	LOAD TAC GATE	16	+	B11-9	SS MODE	11	+	B11-54	MD BIT 7	21	-
P10-27	LAMP BUS 8		-	B11-10	SS MODE	11	-	B11-55	COPS+CLEAR	19	-
B10-28	NO CONNECTION	10		B11-11	TCP RESET	11	-	B11-56	MD BIT 2	21	-
B10-29	LAMP BUS 10		-	B11-12	START TCP STB	11	-	B11-57	MD BIT 1	21	-
B10-30	NO CONNECTION	10		B11-13	ADV CS CLOCK	11	+	B11-58	MD BIT 3	21	-
B10-31	ACC BIT 13	10	+	B11-14	LAMP BUS 0		-	B11-59	POWER SUPPLY CONN	11	
B10-32	NO CONNECTION	10		B11-15	LAMP BUS 6		-	B11-60	POWER SUPPLY CONN	11	
B10-33	LAMP BUS 9		-	B11-16	CS LEVEL	11	-	B11-61	POWER SUPPLY CONN	11	
B10-34	EXT BIT 15 SERIAL IN	15	+	B11-17	X 2	11	+	B11-62	POWER SUPPLY CONN	11	
B10-35	LAMP BUS 11		-	B11-18	RUN + SS MODE.	12	-	B12-1	RUN	12	-
B10-36	NO CONNECTION	10		B11-19	CS LEVEL	11	+	B12-2	STOP T CLOCK	19	-
B10-37	GATE LAMPS P8	20	-	B11-20	SET BSI	15	-	B12-3	OP BIT 9	12	-
B10-38	NO CONNECTION	10		B11-21	GATE IXR TO OPR	15	-	B12-4	IXR ADD 0	15	+
B10-39	NO CONNECTION	10		B11-22	T 6	12	+	B12-5	START REQ INT BSI	17	-
B10-40	NO CONNECTION	10		B11-23	HOLD CS ADD (X7)	11	+	B12-6	RUN + SS MODE	12	-
B10-41	ACC BIT 15	10	+	B11-24	DC RESET	19	+	B12-7	START TCP STB	11	-
B10-42	NO CONNECTION	10		B11-25	SBR BIT 0	8	+	B12-8	START REQ P1	19	-
B10-43	GATE MD TO DRG 8-15	16	-	B11-26	X 7	11	+	B12-9	GATE DISP TO DRG	16	-
B10-44	MD BIT 14	21	-	B11-27	SBR BIT 1	8	+	B12-10	OP BIT 6	11	-
B10-45	MD BIT 8	21	-	B11-28	SBR BIT 2	8	+	B12-11	GATE DISP TO TAC	16	-
B10-46	MD BIT 10	21	-	B11-29	SBR BIT 5	8	+	B12-12	OP BIT 7	11	-
B10-47	LAMP BUS 14		-	B11-30	SBR BIT 3	8	+	B12-13	TAG Y = 0	12	-
B10-48	LAMP BUS 12		-	B11-31	MD BIT 4	21	-	B12-14	OP BIT 8	12	-
B10-49	EXT BIT 15	10	+	B11-32	SBR BIT 4	8	+	B12-15	TAG X = 7	12	+
B10-50	EXT BIT 14	10	+	B11-33	NO CONNECTION	11		B12-16	TAG X = 0	12	+
B10-51	LAMP BUS 15		-	B11-34	PARITY 0-7 EVEN	11	+	B12-17	OP BIT 11	12	-
B10-52	MD BIT 9	21	-	B11-35	GATE MD TO OPR	15	+	B12-18	OP BIT 15	12	-
B10-53	LAMP BUS 13		-	B11-36	LAST I	17	-	B12-19	OP BIT 10	12	-
B10-54	MD BIT 13	21	-	B11-37	S CYCLE S-112	22	-	B12-20	NO CONNECTION	12	
B10-55	MD BIT 11	21	-	B11-38	XIO	17	-	B12-21	OP BIT 14	12	-
B10-56	MD BIT 15	21	-	B11-39	NO CONNECTION	11		B12-22	MD BIT 14	21	-
B10-57	MD BIT 12	21	-	B11-40	MD BIT 6	21	-	B12-23	MD BIT 9	21	-
B10-58	NO CONNECTION	10		B11-41	MD BIT 0	21	-	B12-24	SET BSI	15	-
P10-59	POWER SUPPLY CONN	10		B11-42	CS REQUEST	18	+	B12-25	DIV CMP HOLD T7	13	-
B10-60	POWER SUPPLY CONN	10		B11-43	SLC HOLD T7	13	-	B12-26	T 2	12	+
B10-61	POWER SUPPLY CONN	10		B11-44	GATE I/O TO BUS	12	-	B12-27	MPY HOLD T7	17	-
B10-62	POWER SUPPLY CONN	10		B11-45	CS ERR CHK STP	19	-	B12-28	MPY SHIFT	13	-
B11-1	LAMP BUS 2		-	B11-46	MD BIT 5	21	-	B12-29	SHOP SHIFT	13	-
B11-2	S STEP S-112	22	-	B11-47	SP BIT	19	+	B12-30	LOAD IXR 8-15 GATE	16	-
B11-3	SBR BIT 7	8	+	B11-48	SHOP SHIFT	13	-	B12-31	GATE MD TO OPR	15	+
B11-4	LAMP BUS 3		-	B11-49	CD BIT 16	11	-	B12-32	SLC HOLD T7	13	-
B11-5	SBR BIT 6	8	+	B11-50	T 7	12	-	B12-33	TAG Y = 7	12	-
B11-6	RST EXTEND	18	+	B11-51	I/F BLOCK CLOCK	21	-	B12-34	CS HOLD T7	11	-
B11-7	E3 CYCLE	17	+	B11-52	SYSCP REF P1	11	-	B12-35	RESET OPR	15	-
B11-8	LAMP BUS 1		-	B11-53	SYSCP REF P2	11	-	B12-36	GATE IXR TO OPR	15	-

DASH: ----------

FILE NUMBER: ----------

DRAWN: I. DRAW

ORIGINATOR: TOM WALTERS

CHECKED: A. FREDELL

1ST/REV RLSE APPROVAL: J. ROYER

1ST RLSED:

REV RLSED: 8-8-75

COMPUTER HARDWARE INC.

TYPE-SIZE: SA

DWG. NO.: 2342

REV.: E

TITLE: SIGNAL LIST 2131 CPU CAGE

SHEET: 37 OF 42

POINT LIST

POINT	SIGNAL			POINT	SIGNAL			POINT	SIGNAL		
B12-37	ADV CS CLOCK	11	+	B13-20	BUS BIT 8		+	B14-3	I/F IN BIT 12		-
B12-38	NO CONNECTION	12		B13-21	DIV	17	-	B14-4	DES 13	22	-
B12-39	OP BIT 12	12	-	B13-22	11 CYCLE	17	-	B14-5	CES 13	XX	-
B12-40	SYSCP REF P1	11	-	B13-23	MPY SHIFT	13	-	B14-6	I/F IN BIT 13		-
B12-41	OP BIT 13	12	-	B13-24	BUS BIT 10		+	B14-7	DES 14	22	-
B12-42	MD BIT 15	21	-	B13-25	CCC = 1	13	-	B14-8	CES 14	XX	-
B12-43	MD BIT 8	21	-	B13-26	OP BIT 13	12	-	B14-9	INT VEC BIT 14	20	-
B12-44	I/O IN BIT 9	14	+	B13-27	RROP	17	+	B14-10	I/O IN BIT 4	14	+
B12-45	I/O IN BIT 15	14	+	B13-28	LAST M	XX	+	B14-11	I/F IN BIT 15		-
B12-46	BUS BIT 12		+	B13-29	GATE CCC TO IXR	13	+	B14-12	SBR BIT 10	9	+
B12-47	MD BIT 11	21	-	B13-30	CCC = J	13	-	B14-13	POLL	18	+
B12-48	I/O IN BIT 11	14	+	B13-31	NO E CYCLE	17	+	B14-14	I/O IN BIT 14	14	+
B12-49	I/O IN BIT 10	14	+	B13-32	BUS BIT 11		+	B14-15	SBR BIT 8	9	+
B12-50	I/O IN BIT 13	14	+	B13-33	BUS BIT 14		+	B14-16	INT VEC BIT 13	20	-
B12-51	I/O IN BIT 14	14	+	B13-34	DIV OVFL RST CCC	15	+	B14-17	I/O IN BIT 6	14	+
B12-52	I/O IN BIT 12	14	+	B13-35	ADV CS CLOCK	11	+	B14-18	CES 15	XX	-
B12-53	BUS BIT 14		+	B13-36	SPARE	13		B14-19	DES 15	22	-
B12-54	PHASE A REF	11	-	B13-37	BUS BIT 13		+	B14-20	I/F IN BIT 6		-
B12-55	I/O IN BIT 8	14	+	B13-38	MPY	17	-	B14-21	I/F IN BIT 14		-
B12-56	MD BIT 12	21	-	B13-39	BUS BIT 15		+	B14-22	DXFR	18	+
B12-57	MD BIT 13	21	-	B13-40	GATE LAMPS P2	20	-	B14-23	AREA 0	18	-
B12-58	MD BIT 10	21	-	B13-41	E2 CYCLE	17	+	B14-24	E3 DXFR	18	+
B12-59	POWER SUPPLY CONN	12		B13-42	BUS BIT 12		+	B14-25	END OP	17	+
B12-60	POWER SUPPLY CONN	12		B13-43	GATE LAMPS P5	20	-	B14-26	E2 DXFR	16	+
B12-61	POWER SUPPLY CONN	12		B13-44	LAMP BUS 4		-	B14-27	NO CONNECTION	14	
B12-62	POWER SUPPLY CONN	12		B13-45	GATE DIV OVFL T7	13	+	B14-28	ERROR CHK	19	-
B13-1	CARRY	13	-	B13-46	BUS BIT 9		+	B14-29	NO CONNECTION	14	
B13-2	T 7	12	-	B13-47	LAMP BUS 16		-	B14-30	ENOP 6	XX	-
B13-3	T 6	12	-	B13-48	ADDOP	17	+	B14-31	TRACE S-112	22	-
B13-4	T 4	12	-	B13-49	BSI	17	-	B14-32	XIO	17	-
B13-5	DC RESET P1	19	-	B13-50	SUBOP	17	+	B14-33	OP BIT 10	12	-
B13-6	DIV E	15	+	B13-51	BSC	17	-	B14-34	BSI	17	-
B13-7	MPY SHIFT	13	+	B13-52	LAMP BUS 2		-	B14-35	NO CONNECTION	14	
B13-8	MPY E1	15	+	B13-53	LAMP BUS 17		-	B14-36	LDX OP BIT 10	14	-
B13-9	SLCOP	17	+	B13-54	LAMP BUS 0		-	B14-37	INH INTERRUPT	14	+
B13-10	ILLOPS	17	-	B13-55	GATE STAT TO SBR	16	-	B14-38	NO CONNECTION	14	
B13-11	T 0	12	-	B13-56	LAMP BUS 1		-	B14-39	ENAB SAR BIT 0	14	+
B13-12	TAG	11	+	B13-57	LAMP BUS 5		-	B14-40	NO CONNECTION	14	
B13-13	OVERFLOW	13	-	B13-58	LAMP BUS 3		-	B14-41	SYSCP REF P1	11	-
B13-14	T 3	12	-	B13-59	POWER SUPPLY CONN	13		B14-42	T 6	12	-
B13-15	DIV CMP HOLD T7	13	-	B13-60	POWER SUPPLY CONN	13		B14-43	NO LVL ACT	20	+
B13-16	NO EA OP	17	-	B13-61	POWER SUPPLY CONN	13		B14-44	ADV CS CLOCK	11	+
B13-17	DIV CMP HOLD T7	13	+	B13-62	POWER SUPPLY CONN	13		B14-45	DC RESET P1	19	-
B13-18	SYSCP REF P1	11	-	B14-1	DES 12	22	-	B14-46	ENDOP EARLY	17	+
B13-19	SKIP COND	15	+	B14-2	I/O IN BIT 13	14	+	B14-47	NO CONNECTION	14	

DASH ---

FILE NUMBER ----------

DRAWN I. DRAW

ORIGINATOR TOM WALTERS

CHECKED A. FREDELL

1ST/REV RLSE APPROVAL J. ROYER

1ST RLSED

REV RLSED 8-8-75

COMPUTER HARDWARE INC

TYPE-SIZE SA

DWG. NO. 2342

REV. E

TITLE SIGNAL LIST 2131 CPU CAGE

SHEET 38 OF 42

POINT LIST

POINT	SIGNAL		POINT	SIGNAL		POINT	SIGNAL	
B14-48	OP BIT 11	12 -	B15-31	DRG BIT 0	10 +	B16-14	DBL PREC OP	17 +
B14-49	COPS+CLEAR	19 -	B15-32	OP BIT 6	11 -	B16-15	RST TAC	16 -
B14-50	INT DISABLE S-109	22 -	B15-33	DIFF SIGN	13 +	B16-16	LOAD IXR 0- 7 GATE	16 -
B14-51	OP BIT 5	11 -	B15-34	DIV OVFL RST CCC	15 +	B16-17	ADV IAR GATE	16 +
B14-52	TAG	11 -	B15-35	OVERFLOW ENAB SET	15 +	B16-18	LOAD IAR GATE	16 -
B14-53	NO CONNECTION	14	B15-36	OP BIT 7	11 -	B16-19	DIV CMP HOLD T7	13 +
B14-54	LDX	17 -	B15-37	OP BIT 8	12 -	B16-20	GATE MD TO DRG 8-15	16 -
B14-55	NO CONNECTION	14	B15-38	OP BIT 5	11 +	B16-21	OP BIT 0	11 -
B14-56	START REQ INT BSI	17 -	B15-39	T 5	12 -	B16-22	COMP LESS OR EQUAL	13 +
B14-57	LAST I	17 -	B15-40	GATE DIV OVFL T7	13 +	B16-23	T 5	12 -
B14-58	NO CONNECTION	14	B15-41	CCC = 0	13 -	B16-24	GATE ALU TO ACC	16 -
B14-59	POWER SUPPLY CONN	14	B15-42	GATE SBR TO CCC	13 -	B16-25	SYSCP REF P2	11 -
B14-60	POWER SUPPLY CONN	14	B15-43	T 7	12 -	B16-26	I1 CYCLE	17 -
B14-61	POWER SUPPLY CONN	14	B15-44	DRG = 0	10 -	B16-27	SENSE OP	18 -
B14-62	POWER SUPPLY CONN	14	B15-45	ALU CARRY OUT	13 +	B16-28	LOAD IXR 8-15 GATE	16 -
B15-1	EOR	17 -	B15-46	BSI	17 -	B16-29	OP BIT 9	12 -
B15-2	SET BSI	15 -	B15-47	MAR BIT 15	9 +	B16-30	INT BSI I1 I2	17 +
B15-3	X 0	11 -	B15-48	IXR ADD 0	15 +	B16-31	BSC	17 -
B15-4	ACC BIT 0	10 +	B15-49	SYSCP REF P2	11 -	B16-32	E CYCLES	17 -
B15-5	MPY E1	15 +	B15-50	T 2	12 -	B16-33	READ	18 -
B15-6	COPS+CLEAR	19 -	B15-51	ALU BIT 0	10 +	B16-34	T0 + X0 RESET	19 -
B15-7	E1 CYCLE	17 -	B15-52	T 1	12 -	B16-35	T 7	12 -
B15-8	T 4	12 -	B15-53	GATE SBR TO BUS	15 -	B16-36	CLEAR BUS T7	19 -
B15-9	XPY	17 -	B15-54	SPARE	15	B16-37	LDOP	17 +
B15-10	OP BIT 9	12 -	B15-55	GATE SBR TO IXR P1	16 -	B16-38	SKIP COND	15 +
B15-11	DIV E1	15 +	B15-56	GATE SBR TO IXR P2	16 -	B16-39	X 1	11 +
B15-12	EXT BIT 15	10 +	B15-57	T 3	12 -	B16-40	GATE SBR TO IXR P1	16 -
B15-13	DIV	17 -	B15-58	ACC BIT 1	10 +	B16-41	E1 CYCLE	17 -
B15-14	ZERO REM	15 +	B15-59	POWER SUPPLY CONN	15	B16-42	GATE ALU TO BUS	16 -
B15-15	GATE IXR TO OPR	15 -	B15-60	POWER SUPPLY CONN	15	B16-43	DC RESET P1	19 -
B15-16	QUOT CORR	13 +	B15-61	POWER SUPPLY CONN	15	B16-44	GATE IAR TO BUS	16 -
B15-17	EXT BIT 15 SERIAL IN	15 +	B15-62	POWER SUPPLY CONN	15	B16-45	T 0	12 -
B15-18	ALU SUB	15 +	B16-1	COPS+CLEAR	19 -	B16-46	STD	17 -
B15-19	EMCSL 123	9 -	B16-2	STS	17 +	B16-47	MPY E1	15 +
B15-20	SUBOP	17 +	B16-3	I2 CYCLE	17 -	B16-48	BSI	17 -
B15-21	IXR ADD 2	15 +	B16-4	RST DRG	16 +	B16-49	E3 CYCLE	17 +
B15-22	MAR BIT 14	9 +	B16-5	GATE KDR TO IAR	19 -	B16-50	MDX	17 +
B15-23	DIV E	15 +	B16-6	BSIE	17 +	B16-51	ZERO REM	15 +
B15-24	ACC BIT 0 = DRG BIT 0	15 -	B16-7	T 2	12 -	B16-52	STX	17 -
B15-25	T 6	12 -	B16-8	COMP EQUAL	13 +	B16-53	CMPOP	17 +
B15-26	OP BIT 12	12 -	B16-9	GATE EXT TO BUS	16 -	B16-54	SPARE	16
B15-27	ALU OVFL	15 +	B16-10	T 6	12 -	B16-55	INH ALU TO ACC	13 +
B15-28	NO CONNECTION	15	B16-11	LAST I	17 -	B16-56	OP BIT 5	11 +
B15-29	TAC BIT 0	10 +	B16-12	MDX SKIP	13 +	B16-57	CCC = 1	13 -
B15-30	ACC BIT 15 SERIAL IN	15 +	B16-13	XIO	17 -	B16-58	RST ACC	16 -

DASH: ----------

FILE NUMBER: ----------

DRAWN: I. DRAW

ORIGINATOR: TOM WALTERS

CHECKED: A. FREDELL

1ST/REV RLSE APPROVAL: J. ROYER

1ST RLSED:

REV RLSED: 8-8-75

COMPUTER HARDWARE INC.

TYPE-SIZE: SA

DWG. NO.: 2342

REV.: E

TITLE: SIGNAL LIST 2131 CPU CAGE

POINT LIST

POINT	SIGNAL			POINT	SIGNAL			POINT	SIGNAL		
B16-59	POWER SUPPLY CONN	16		B17-42	OP BIT 5	11	-	B18-25	X 2	11	+
B16-60	POWER SUPPLY CONN	16		B17-43	X 2	11	+	B18-26	SBR BIT 0	8	+
B16-61	POWER SUPPLY CONN	16		B17-44	TAG	11	-	B18-27	X 6	11	+
B16-62	POWER SUPPLY CONN	16		B17-45	INT ACK	17	-	B18-28	CONTROL	18	-
B17-1	DIV	17	-	B17-46	E3 CYCLE	17	+	B18-29	X 4	11	+
B17-2	MPY	17	-	B17-47	NO E CYCLE	17	+	B18-30	SBR BIT 2	8	+
B17-3	FLT	17	-	B17-48	READ	18	-	B18-31	T 7	12	-
B17-4	EOR	17	-	B17-49	STS	17	+	B18-32	READ	18	-
B17-5	STX	17	-	B17-50	I/F CS DATA STORE	21	-	B18-33	DC RESET P2	19	-
B17-6	OR	17	-	B17-51	SEL HEXD A	17	+	B18-34	WRITE	18	-
B17-7	STO	17	-	B17-52	COPS DISP CYCLE	19	-	B18-35	READ+WRITE	18	+
B17-8	MDM	17	+	B17-53	T 0	12	-	B18-36	SENSE DEV	18	-
B17-9	AND	17	-	B17-54	T 5	12	-	B18-37	X 7	11	+
B17-10	OP BIT 0	11	-	B17-55	GATE I/O TO SBR	17	-	B18-38	E2 CYCLE	17	+
B17-11	COPS+CLEAR	19	-	B17-56	INDST	17	-	B18-39	AREA 7	18	-
B17-12	WAIT	17	-	B17-57	SLCOP	17	+	B18-40	AC PWR ON RESET	XX	-
B17-13	ILLOPS	17	-	B17-58	SAR CMP S-112	22	-	B18-40	NO CONNECTION	18	
B17-14	ENDOP EARLY	17	+	B17-59	POWER SUPPLY CONN	17		B18-41	RST EXTEND	18	+
B17-15	CCC = 0	13	-	B17-60	POWER SUPPLY CONN	17		B18-42	X 1	11	+
B17-16	BSC	17	-	B17-61	POWER SUPPLY CONN	17		B18-43	SBR BIT 8	9	+
B17-17	DIOP	17	-	B17-62	POWER SUPPLY CONN	17		B18-44	X 3	11	-
B17-18	SHOPS	17	+	B18-1	AREA 0	18	-	B18-45	T 3	12	-
B17-19	MAR CMP	9	-	B18-2	POLL INT	18	+	B18-46	T 1	12	-
B17-20	CS LEVEL	11	+	B18-3	I/F OUT BIT 2	18	-	B18-47	I/F OUT BIT 8	18	-
B17-21	SENSE OP	18	-	B18-4	T 4	12	-	B18-48	I/F DC RESET	18	-
B17-22	CPU CLOCK	17	-	B18-5	SBR BIT 14	9	+	B18-49	SBR BIT 6	8	+
B17-23	OP BIT 1	11	-	B18-6	I/F POLL	18	-	B18-50	T 5	12	-
B17-24	OP BIT 2	11	-	B18-7	SBR BIT 12	9	+	B18-51	I/F OUT BIT 6	18	-
B17-25	GATE LAMPS P7	20	-	B18-8	T 2	12	-	B18-52	X 5	11	+
B17-26	IAR CMP S-112	22	-	B18-9	I/F OUT BIT 14	18	-	B18-53	I/F CLOCK	18	-
B17-27	LDS	17	+	B18-10	I/F OUT BIT 12	18	-	B18-54	NO CONNECTION	18	
B17-28	HEXD ENAB	17	-	B18-11	SBR BIT 10	9	+	B18-55	NO CONNECTION	18	
B17-29	INH PAR CHK ON INT	17	-	B18-12	SBR BIT 4	8	+	B18-56	NO CONNECTION	18	
B17-30	WRITE	18	-	B18-13	I/F OUT BIT 10	18	-	B18-57	NO CONNECTION	18	
B17-31	RROP	17	-	B18-14	I/F OUT BIT 0	18	-	B18-58	NO CONNECTION	18	
B17-32	SKIP COND	15	+	B18-15	DXFR	18	+	B18-59	POWER SUPPLY CONN	18	
B17-33	RROP	17	+	B18-16	I/F OUT BIT 4	18	-	B18-60	POWER SUPPLY CONN	18	
B17-34	OP BIT 4	11	-	B18-17	ENOP 2	XX	+	B18-61	POWER SUPPLY CONN	18	
B17-35	OP BIT 3	11	-	B18-18	E3 CYCLE	17	+	B18-62	POWER SUPPLY CONN	18	
B17-36	RESET INT	17	-	B18-19	I/F DXFR	18	-	B19-1	STOP S-301	22	-
B17-37	NO EA OP	17	-	B18-20	CS REQUEST	18	+	B19-2	START S-302	22	-
B17-38	MDX	17	+	B18-21	E2 DXFR	18	+	B19-3	IMM STOP S-305	22	-
B17-39	GATE DES TO I/O	19	-	B18-22	E1 CYCLE	17	-	B19-4	KEY E	22	-
B17-40	LDX	17	-	B18-23	E3 DXFR	18	+	B19-5	KEY F	22	-
B17-41	T 2	12	-	B18-24	T 6	12	-	B19-6	RESET S-308	22	-

DATA: ---------- | FILE NUMBER: ----------

DRAWN: I. DRAW | ORIGINATOR: TOM WALTERS

CHECKED: A. FREDELL | 1ST/REV RLSE APPROVAL: J. ROYER

1ST RLSED | REV RLSED: 8-8-75

COMPUTER HARDWARE INC.

TYPE-SIZE: SA | DWG. NO.: 2342 | REV.: E | TITLE: SIGNAL LIST 2131 CPU CAGE | SHEET: 40 OF 42

POINT LIST

POINT	SIGNAL			POINT	SIGNAL			POINT	SIGNAL		
B19-7	OP BIT 15	12	-	B19-52	LAMP BUS 17		-	B20-35	INT REQ 0		-
B19-8	WRT STG PRT S-110	22	-	B19-53	STOP T CLOCK	19	-	B20-36	LAMP CLOCK	20	+
B19-9	GATE DES TO I/O	19	-	B19-54	SP BIT	19	-	B20-37	INT REQ 3		-
B19-10	DC RESET	19	+	B19-55	ENDOP EARLY	17	+	B20-38	I/F IN BIT 5		-
B19-11	RUN S-112	22	-	B19-56	INH PAR CHK ON INT	17	-	B20-39	NO CONNECTION	20	
B19-12	T 2	12	+	B19-57	T 1	12	-	B20-40	NO CONNECTION	20	
B19-13	IMM STOP	19	+	B19-58	START REQ INT BSI	17	-	B20-41	INT REQ 2		-
B19-14	GATE KDR TO SBR	19	-	B19-59	POWER SUPPLY CONN	19		B20-42	SBR BIT 8	9	+
B19-15	PWR ON RST	18	-	B19-60	POWER SUPPLY CONN	19		B20-43	END OP	17	+
B19-16	ENOP 5	XX	+	B19-61	POWER SUPPLY CONN	19		B20-44	NO CONNECTION	20	
B19-17	DC RESET P1	19	-	B19-62	POWER SUPPLY CONN	19		B20-45	INT ACK	17	-
B19-18	STOP	19	+	B20-1	SBR BIT 15	9	+	B20-46	NO CONNECTION	20	
B19-19	TRACE	19	+	B20-2	I/F IN BIT 2		-	B20-47	NO CONNECTION	20	
B19-20	START TCP STB	11	-	B20-3	POLL INT	18	+	B20-48	T 6	12	-
B19-21	PROG STOP	19	-	B20-4	INT VEC BIT 12	20	+	B20-49	NO CONNECTION	20	
B19-22	OP BIT 9	12	-	B20-5	INT VEC BIT 12	20	-	B20-50	CONTROL	18	-
B19-23	CLOCK SBR 0- 7	19	+	B20-6	I/F IN BIT 0		-	B20-51	AREA 7	18	-
B19-24	CMP CHK	17	-	B20-7	SBR BIT 1	8	+	B20-52	INT VEC BIT 0	20	-
B19-25	ILLOPS	17	-	B20-8	INT VEC BIT 13	20	-	B20-53	SBR BIT 9	9	+
B19-26	LOAD SBR GATE	10	+	B20-9	NO LVL ACT	20	+	B20-54	NO CONNECTION	20	
B19-27	S INST S-112	22	-	B20-10	SBR BIT 0	8	+	B20-55	NO CONNECTION	20	
B19-28	CLOCK SBR 8-15	19	+	B20-11	INT VEC BIT 13	20	+	B20-56	NO CONNECTION	20	
B19-29	MD BIT 17	21	-	B20-12	NO CONNECTION	20		B20-57	NO CONNECTION	20	
B19-30	TRACE S-112	22	-	B20-13	SBR BIT 14	9	+	B20-58	NO CONNECTION	20	
B19-31	DISP/SP S-112	22	-	B20-14	NO CONNECTION	20		B20-59	POWER SUPPLY CONN	20	
B19-32	COPS DISP CYCLE	19	-	B20-15	I/F IN BIT 1		-	B20-60	POWER SUPPLY CONN	20	
B19-33	T 4	12	-	B20-16	PROG STOP	19	-	B20-61	POWER SUPPLY CONN	20	
B19-34	COPS LOAD CYCLE	19	-	B20-17	SENSE DEV	18	-	B20-62	POWER SUPPLY CONN	20	
B19-35	START CLOCK	19	+	B20-18	TRACE	19	+	B21-1	I/F OUT BIT 1	18	-
B19-36	ERROR CHK	19	-	B20-19	I/F IN BIT 1		-	B21-2	I/F IN BIT 1		-
B19-37	COPS+CLEAR	19	-	B20-20	NO CONNECTION	20		B21-3	NO CONNECTION	21	
B19-38	GATE STAT TO SBR	16	-	B20-21	INT REQ 1		-	B21-4	I/F DC RESET	18	-
B19-39	CHECK STOP S-111	22	-	B20-22	I/F IN BIT 6		-	B21-5	I/F IN BIT 5		-
B19-40	CS ERR CHK STP	19	-	B20-23	INT REQ A		-	B21-6	I/F PROG LOAD BUSY	21	-
B19-41	STSE	17	+	B20-24	I/F IN BIT 0		-	B21-7	I/F BLOCK CLOCK	21	-
B19-42	SPARE	19		B20-25	E2 DXFR	18	+	B21-8	I/F CS REQ	21	-
B19-43	I1 CYCLE	17	-	B20-26	PHASE A REF	11	-	B21-9	I/F IN BIT 2		-
B19-44	GATE LAMPS P7	20	-	B20-27	I/F IN BIT 4		-	B21-10	I/F RESET EXTEND	21	-
B19-45	COND RUN	17	+	B20-28	NO CONNECTION	20		B21-11	I/F IN BIT 6		-
B19-46	X 7	11	+	B20-29	INT REQ 4		-	B21-12	I/F IN BIT 0		-
B19-47	LAMP BUS 7		-	B20-30	I/F IN BIT 5		-	B21-13	I/F IN BIT 3		-
B19-48	GATE LAMPS P1	20	-	B20-31	INT REQ 5		-	B21-14	I/F PWR ON RST	18	-
B19-49	SP BIT	19	+	B20-32	I/F IN BIT 7		-	B21-15	I/F IN BIT 4		-
B19-50	LAMP BUS 16		-	B20-33	NO CONNECTION	20		B21-16	I/F E2+E3	18	+
B19-51	SBR PARITY ODD	12	-	B20-34	INT REQ B		-	B21-17	I/F CLOCK	18	-

SIGNAL LIST 2131 CPU CAGE

TYPE-SIZE	DWG. NO.	REV.	TITLE	SHEET
SA	2342	E		41 OF 42

DASH			
FILE NUMBER			
ORIGINATOR TOM WALTERS	DRAWN I. DRAW	CHECKED A. FREDELL	1ST RLSD
1ST/REV RLSE APPROVAL J. ROYER			REV RLSED 8-8-75

COMPUTER HARDWARE INC.

POINT LIST

POINT	SIGNAL			POINT	SIGNAL			POINT	SIGNAL		
B21-18	I/F CPU CLOCK	18	+	B22-1	DES 13	22	-	B22-46	KEY D	22	-
B21-19	I/F E1+E3	18	+	B22-2	DES 14	22	-	B22-47	KEY B	22	-
B21-20	I/F OUT BIT 9	18	-	B22-3	DES 12	22	-	B22-48	KEY C	22	-
B21-21	I/F CS CYCLE	18	-	B22-4	DES 15	22	-	B22-49	CMP CHK IND	17	-
B21-22	I/F OUT BIT 0	18	-	B22-5	LAMP CLOCK	20	+	B22-50	KEY E	22	-
B21-23	I/F OUT BIT 11	18	-	B22-6	LAMP BUS 12		-	B22-51	HEX BIT 12	9	+
B21-24	I/F INH CS REQ	18	+	B22-7	LAMP MPX A	20	+	B22-52	KEY F	22	-
B21-25	I/F OUT BIT 8	18	-	B22-8	LAMP BUS 6		-	B22-53	HEX BIT 14	9	+
B21-26	I/F CS DATA STORE	21	-	B22-9	S INST S-112	22	-	B22-54	KEY 8	22	-
B21-27	I/F IN BIT 9		-	B22-10	LAMP BUS 13		-	B22-55	HEX BIT 9	9	+
B21-28	I/F OUT BIT 4	18	-	B22-11	TRACE S-112	22	-	B22-56	KEY 9	22	-
B21-29	I/F IN BIT 15		-	B22-12	LAMP BUS 11		-	B22-57	HEX BIT 4	8	+
B21-30	I/F POLL	18	-	B22-13	IAR CMP S-112	22	-	B22-58	HEX BIT 6	8	+
B21-31	I/F OUT BIT 10	18	-	B22-14	LAMP BUS 14		-	B22-59	POWER SUPPLY CONN	22	
B21-32	I/F OUT BIT 3	18	-	B22-15	CONSOLE S-112	22	-	B22-60	POWER SUPPLY CONN	22	
B21-33	I/F IN BIT 10		-	B22-16	LAMP BUS 10		-	B22-61	POWER SUPPLY CONN	22	
B21-34	I/F OUT BIT 5	18	-	B22-17	RUN S-112	22	-	B22-62	POWER SUPPLY CONN	22	
B21-35	I/F IN BIT 11		-	B22-18	LAMP BUS 9		-				
B21-36	I/F FUNC CLEAR	18	-	B22-19	IMM STOP S-305	22	-				
B21-37	I/F PARITY ERR	18	-	B22-20	SELECT DISPLAY 1	XX	+				
B21-38	I/F OUT BIT 7	18	-	B22-21	PROG LOAD S-311	22	-				
B21-39	NO CONNECTION	21		B22-22	LAMP MPX B	20	+				
B21-40	I/F OUT BIT 6	18	-	B22-23	CLEAR STG S-304	22	-				
B21-41	I/F OUT BIT 12	18	-	B22-24	DES 0	22	-				
B21-42	I/F OXFR	18	-	B22-25	LAMP MPX D	20	+				
B21-43	I/F PHASE A	18	-	B22-26	DES 1	22	-				
B21-44	I/F OUT BIT 14	18	-	B22-27	LAMP MPX C	20	+				
B21-45	I/F OUT BIT 15	18	-	B22-28	LOAD ACC S-309	22	-				
B21-46	I/F PROG LOAD	18	-	B22-29	PROG CTL RST S-300	22	-				
B21-47	I/F IN BIT 14		-	B22-30	LOAD STG S-306	22	-				
B21-48	I/F IN BIT 8		-	B22-31	DISP STG S-303	22	-				
B21-49	I/F IN BIT 7		-	B22-32	LOAD IAR S-300	22	-				
B21-50	NO CONNECTION	21		B22-33	KEY 2	22	-				
B21-51	I/F IN BIT 13		-	B22-34	CONS INT S-310	22	-				
B21-52	NO CONNECTION	21		B22-35	KEY 3	22	-				
B21-53	I/F IN BIT 12		-	B22-36	STOP S-301	22	-				
B21-54	NO CONNECTION	21		B22-37	KEY 4	22	-				
B21-55	I/F OUT BIT 2	18	-	B22-38	START S-302	22	-				
B21-56	I/F OUT BIT 13	18	-	B22-39	KEY 5	22	-				
B21-57	I/F STG PRT ERR	18	-	B22-40	SPARE S-307	22	-				
B21-58	NO CONNECTION	21		B22-41	KEY 6	22	-				
B21-59	NO CONNECTION	21		B22-42	PAR CHK	19	-				
B21-60	NO CONNECTION	21		B22-43	KEY 7	22	-				
B21-61	POWER SUPPLY CONN	21		B22-44	SP CHECK	19	-				
B21-62	POWER SUPPLY CONN	21		B22-45	KEY A	22	-				

DASH ---

FILE NUMBER ---

DRAWN I. DRAW

ORIGINATOR TOM WALTERS

CHECKED A. FREDELL

1ST/REV RLSE APPROVAL J. ROYER

1ST RLSED

REV RLSED 8-8-75

COMPUTER HARDWARE INC.

TYPE-SIZE SA

DWG. NO. 2342

REV. E

TITLE SIGNAL LIST 2131 CPU CAGE

SHEET 42 OF 42

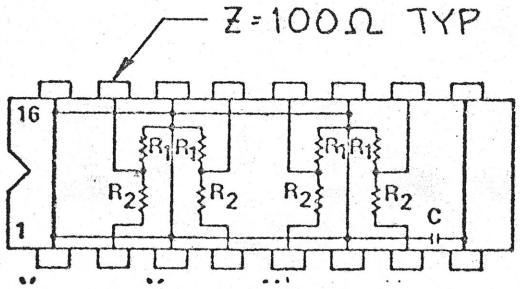
MEMORY CAGE

TYPE-SIZE	DWG. NO.	REV.	TITLE	SHEET
SA	2394	A	CABLE, INTERNAL, CPU TO MEMORY -2131	1 OF 4

FROM	TO	SIGNAL
A21-1	GROUND	
A21-2	GROUND	
A21-3	+5	
A21-4	J1-2	STG ADD 4
A21-5	J1-4	STG ADD 5
A21-6	J1-6	STG ADD 6
A21-7	J1-8	STG ADD 7
A21-8	J1-10	STG ADD 8
A21-9	J1-12	STG ADD 9
A21-10	J1-14	STG ADD 10
A21-11	J1-16	STG ADD 11
A21-12	J1-18	STG ADD 12
A21-13	J1-20	STG ADD 13
A21-14	J1-22	STG ADD 14
A21-15	J1-24	STG ADD 15
A21-16	J1-26	SELECT CSM 1
A21-17	J1-28	SELECT CSM 2
A21-18	J1-30	SELECT CSM 3
A21-19	J1-32	SELECT CSM 4
A21-20	J1-34	SELECT CSM 5
A21-21	J1-36	SELECT CSM 6
A21-22	J1-38	SELECT CSM 7
A21-23	J1-40	SELECT CSM 8
A21-24	J1-42	MEM WRITE
A21-25	J1-44	MEM READ
A21-26	J1-54	CD BIT 0
A21-28	J1-60	CD BIT 1

		DRAWN	CHECKED	1ST RLSED		
		J. ROYER 01/16/75	J. ROYER	01/16/75		COMPUTER HARDWARE INC.
DASH	FILE NUMBER	ORIGINATOR T.W.	1ST/REV RLSE APPROVAL	REV RLSED 03/26/75		

FROM	TO	SIGNAL
A21-30	J1-66	CD BIT 2
A21-32	J1-72	CD BIT 3
A21-34	J1-78	CD BIT 4
A21-36	J1-84	CD BIT 5
A21-38	J2-4	CD BIT 6
A21-40	J2-10	CD BIT 7
A21-42	J2-16	CD BIT 8
A21-44	J2-22	CD BIT 9
A21-46	J2-28	CD BIT 10
A21-48	J2-34	CD BIT 11
A21-50	J2-40	CD BIT 12
A21-52	J2-46	CD BIT 13
A21-54	J2-52	CD BIT 14
A21-56	J2-58	CD BIT 15
A21-58	J2-64	CD BIT 16
A21-59	J2-66	MD BIT 16
A21-60	J2-70	CD BIT 17
A21-61	J2-72	MD BIT 17
A21-62	J2-74	STG ADD 3



IC 2, 3, 10, 13 NETWORK

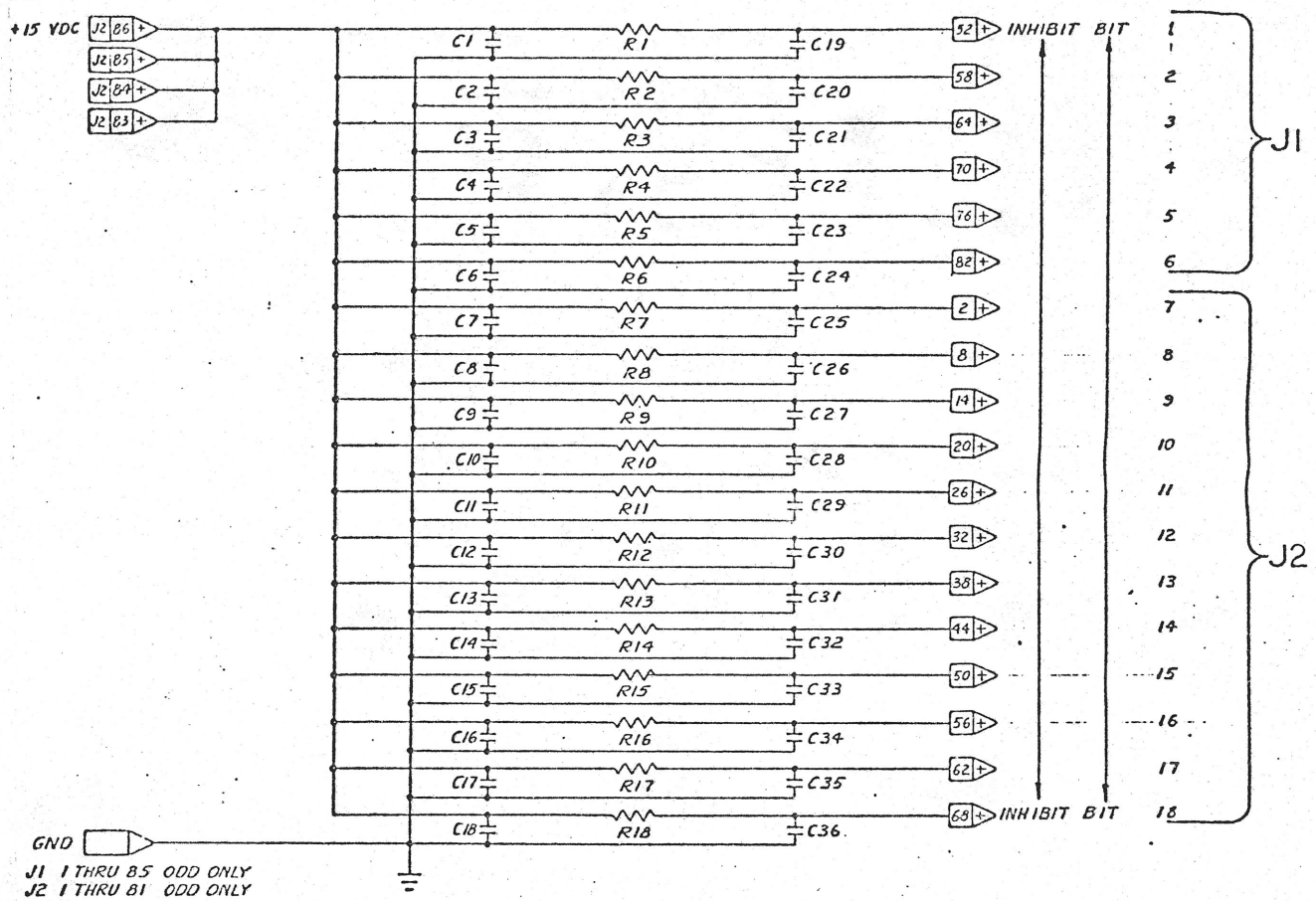
FROM	TO	SIGNAL	TERMINATOR
A21-27	J1-56	MD BIT 0	IC2-13
A21-29	J1-62	MD BIT 1	IC2-15
A21-31	J1-68	MD BIT 2	IC2-12
A21-33	J1-74	MD BIT 3	IC2-10
A21-35	J1-80	MD BIT 4	IC10-15
A21-37	J1-86	MD BIT 5	IC10-13
A21-39	J2-6	MD BIT 6	IC10-12
A21-41	J2-12	MD BIT 7	IC10-10
A21-43	J2-18	MD BIT 8	IC3-15
A21-45	J2-24	MD BIT 9	IC3-13
A21-47	J2-30	MD BIT 10	IC3-12
A21-49	J2-36	MD BIT 11	IC3-10
A21-51	J2-42	MD BIT 12	IC11-15
A21-53	J2-48	MD BIT 13	IC11-13
A21-55	J2-54	MD BIT 14	IC11-12
A21-57	J2-60	MD BIT 15	IC11-10

NOTES:

1. USED WITH CABLE CD-2011.

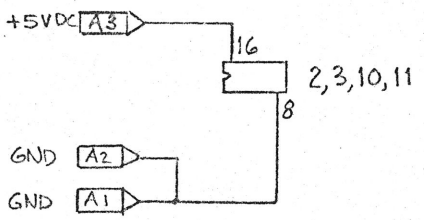
COMPUTER HARDWARE INC.

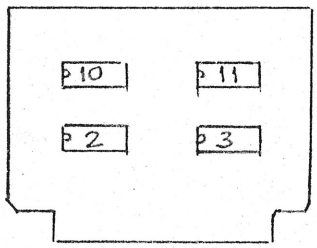
TYPE-SIZE	DWG. NO.	REV.	TITLE	SHEET
SA	2394			4 or 4



REF:
C1 THRU C18 6.8μf 35V.
C19 THRU C36 .0047μf.
R1 THRU R18 13.7Ω 7W 1% NON-INDUCTIVE WW

MEMORY INTERFACE





MEMORY PADDLE

SEE NOTES ON SH. 3

		DRAWN	CHECKED	1ST RLSED	
DASH	FILE NUMBER	ORIGINATOR	1ST/REV. RLSE APPROVAL	REV RLSED	

COMPUTER HARDWARE INC.

CORE MODULE ELECTRONICS

The CM contains the circuitry required to drive and sense the core stack. To function, it requires READ and WRITE pulse inputs to generate read and write memory half cycles, respectively. Timing signals generated within the CM are factory set and should not require readjustment for the life of the equipment.

Timing and Control Signals

1. RTD and RTS are current pulses of durations approximately equal to that of the READ timing pulse input and are used to close selected drive and sink switches in the X and Y stack drive circuits. For example, RTDX closes 1 of 8 read-drive floating switches composed of CR17, T17 and Q26. Address decoder IC13 performs the 1 of 8 switch selection. RTSX, RTDY and RTSY perform in a similar manner.
2. WTD and WTS perform the same function as RTD and RTS, but occur during a write half cycle.
3. Strobe is a short positive pulse to the sense amplifiers which occurs approximately at core peaking time during a read half cycle. Strobe is generated by the timing curcuits associated with Q21, Q22 and Q23.
4. TZ is a timing pulse enabling input data to control the inhibit current switches. The duration of TZ is approximately equal to that of the WRITE pulse input plus 70ns, the delay time of DL2.

X and Y DRIVE CIRCUITS

X and Y drive currents to the core stack are controlled in magnitude and rise time by two linear, active current sources composed of Q14, Q16 and Q19 and associated components. R50 and C19 form an R-C integrator to control current rise times. Q12 clamps the current magnitudes to a value established by the core stack thermistor to provide current-versus-temperature compensation. Current source outputs are routed to stack drive and sink switch transistors at the core stack periphery by an eight-transformer distribution matrix.

DATA CIRCUITS

Core stack signal sensing is performed by a dual-channel integrated circuit sense amplifier (IC6). The sense lines are terminated by R21. Pins 4 and 5 of IC6 are inputs to a reference amplifier which sets the threshold for identical amplifiers at pins 2-3 and 6-7 of the same IC. Signal threshold is developed across R15 by a precision voltage divider network.

The strobe pulse to the sense amplifier gates the sense amplifier at read time and enables data read-out of the core stack to be transferred to the data output buffers, Q5 and Q6. Q5 and Q6 are fast-on, slow-off devices to effectively stretch the $\overline{\text{Memory Data}}$ ($\overline{\text{MD}}$) output pulse width.

Inhibit switches (Darlington pairs Q_1 - Q_3 and Q_2 - Q_4 supply inhibit currents from remote inhibit resistors to the center-tapped sense/inhibit lines. The inhibit switches are controlled by input data, Control Data ($\overline{\text{CD}}$), as timed by TZ during a write cycle.

CORE MODULE MAGNETICS

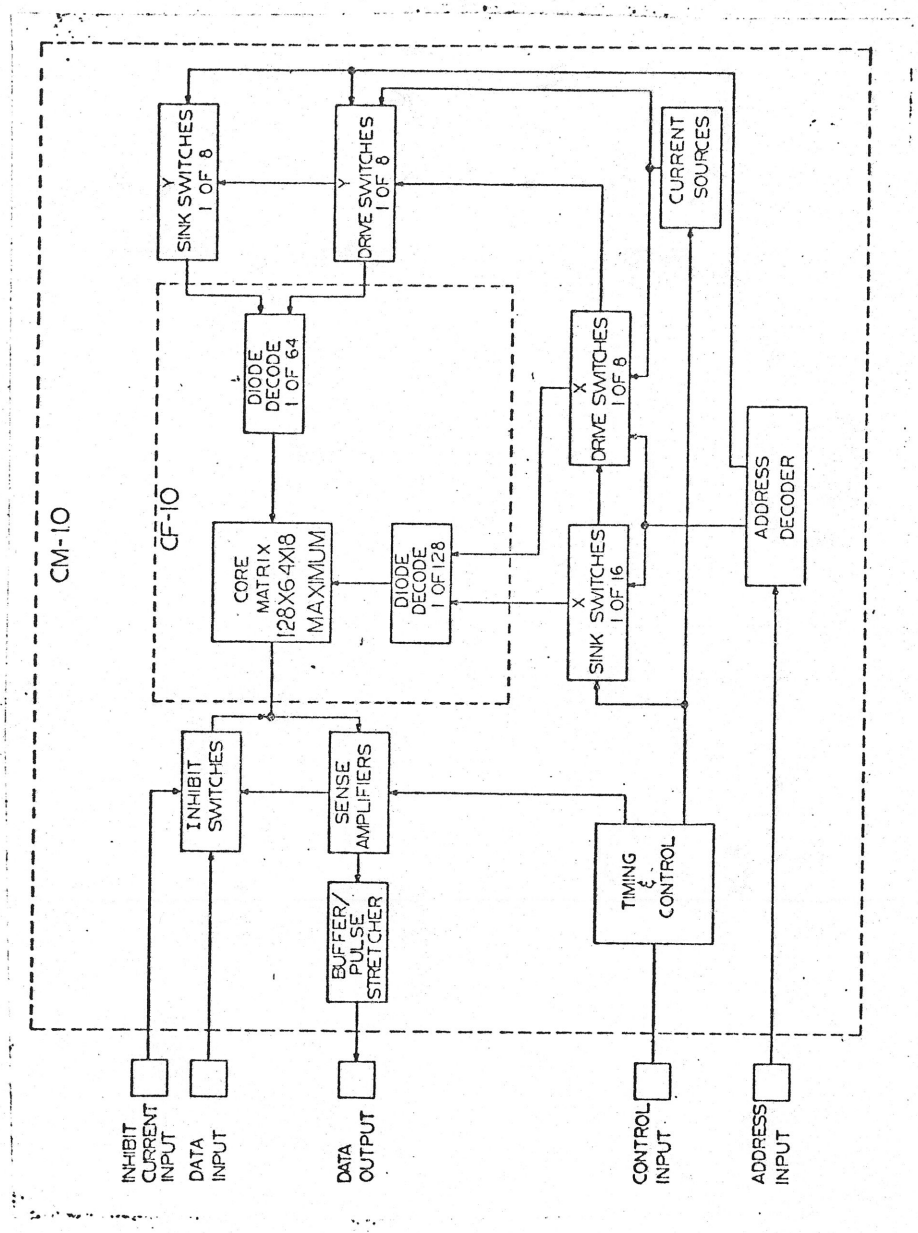
The core stack assembly, mounted centrally on the CM contains the lithium-nickel ferrite core arrays positioned between two hinged P.C. boards. The core arrays are affixed to ground planes between the two boards to minimize thermal gradients in the core area. Diode decode matrices for the X and Y axes are located at the core stack periphery.

A thermistor is provided to sense core temperatures. The thermistor becomes a part of a servo loop in the stack drive electronics to compensate for variations in core characteristics with temperature changes.

The core stack is electrically organized as a 3D, 3 wire coincident-current core stack. A memory data word is addressed for read or write by applying one half of the required core switching current on one selected X line and one half on one selected Y line. There are 128 X axis and 64 Y axis drive lines for a total of 8192 word intersections. The core performs the AND logic function in the address selection process, because only when X and Y currents are present in the core aperture will the core be selected.

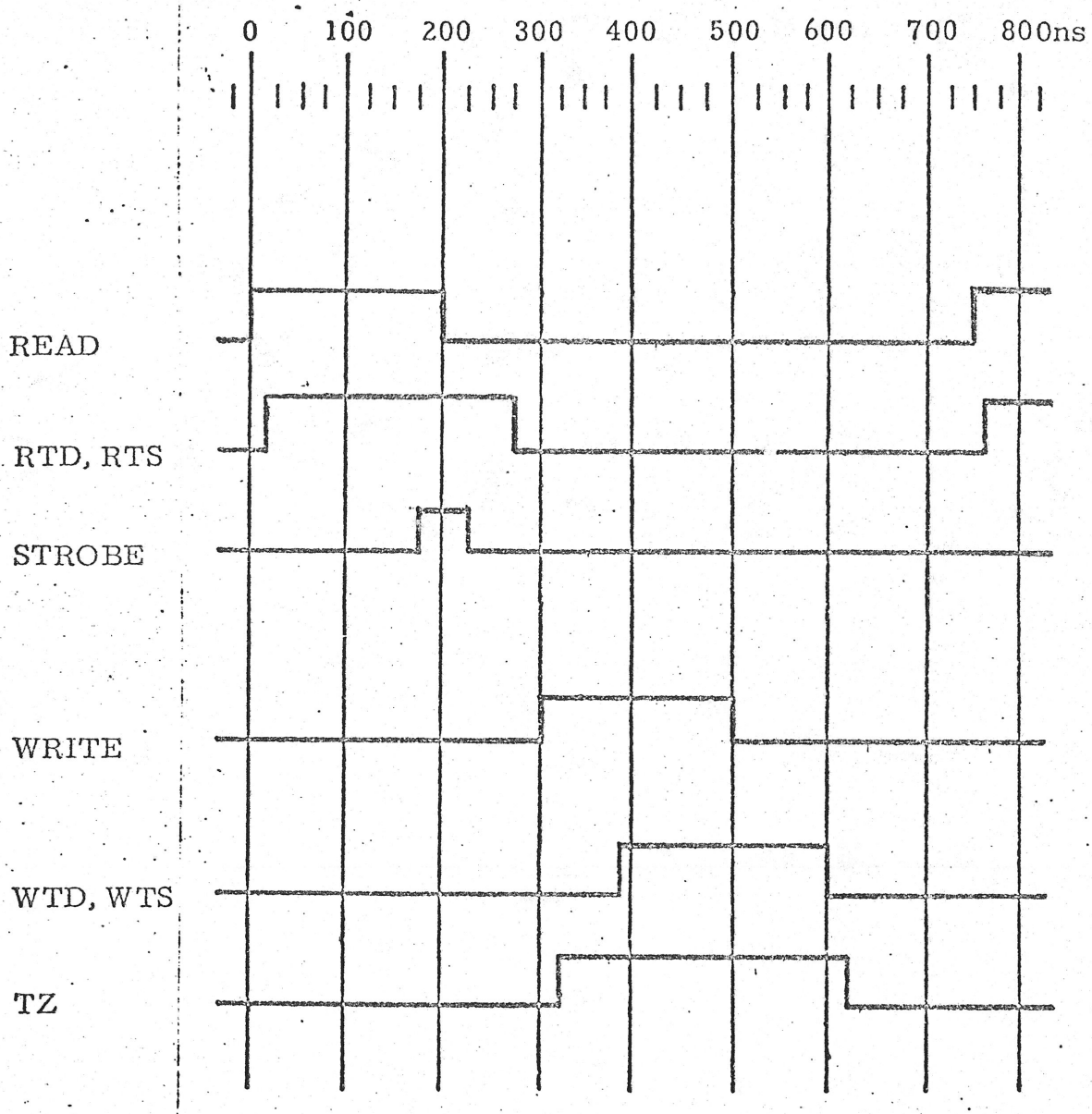
One of 64 drive lines on each axis is selected via an 8 X 8, two-diode-per-line selection matrix. The third line through the memory cores is used as the common sense-inhibit line for the during read time the sense-inhibit line is used to sense the flux reversal in the core. During write time the sense-inhibit line

is used to inhibit the X and Y currents from setting a core to the "1" state, if "0" is to be written. The magnitude and direction of the inhibit current is such that the net magnetic field is not sufficient to flip the core. In effect the "AND gate" (core) is blocked. Conversely, when "1" is to be written, the inhibit line is not energized. Eighteen sense/inhibit lines are used to read and write the data pattern at the location selected by the coincidence of X and Y currents.



CORE MODULE BLOCK DIAGRAM

FIGURE 1



CORE MODULE TIMING DIAGRAM

FIGURE 2

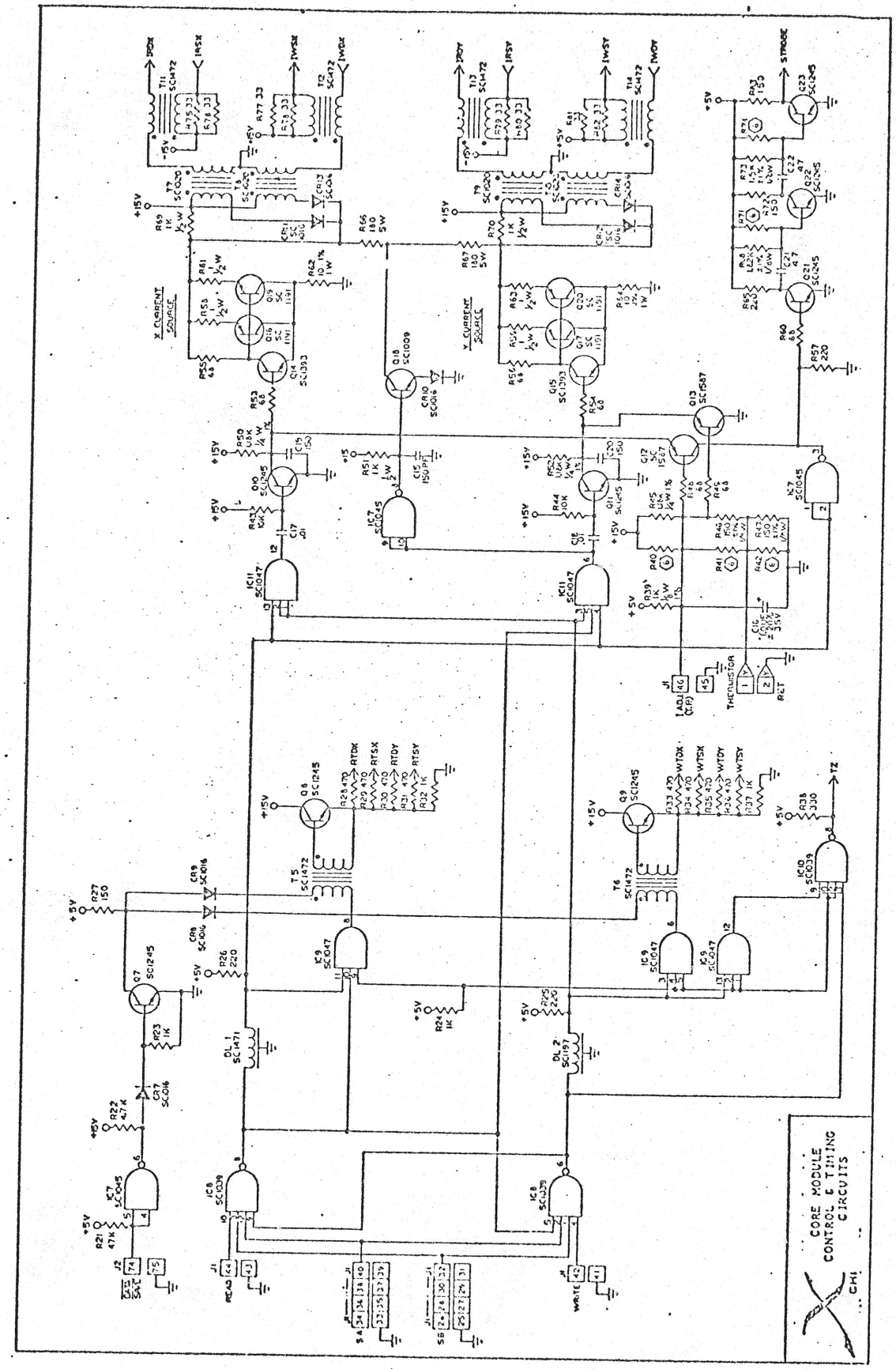


FIGURE 3A 3

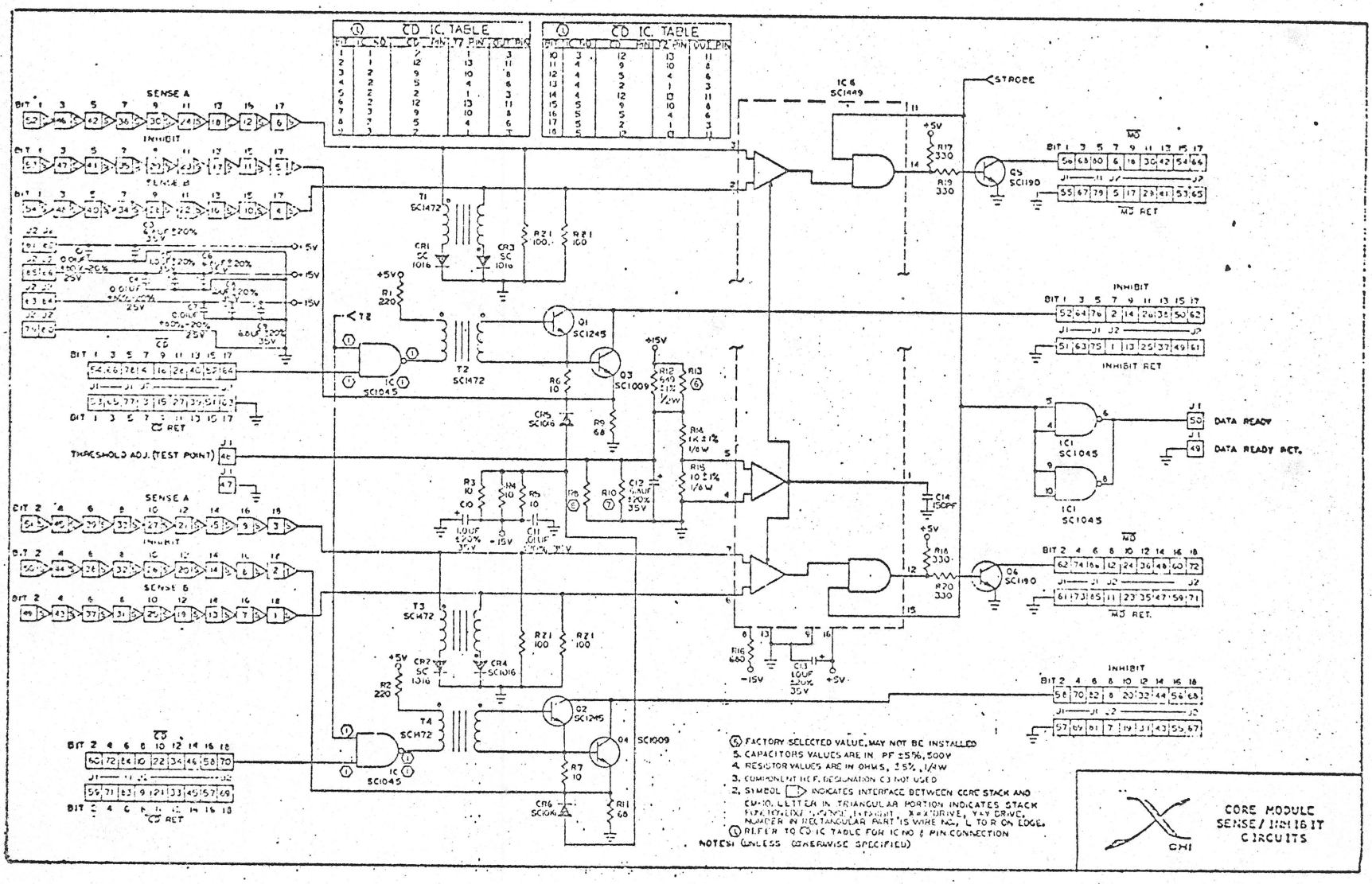

CD IC. TABLE
CD IC. TABLE
SENSE A
INHIBIT
SENSE B
STROBE
IC 6 SC1449
Q5 SC1190
Q6 SC1190
T1 SC1472
T2 SC1472
T3 SC472
T4 SC472
Q1 SC1245
Q2 SC1245
Q3 SC1009
Q4 SC1009
IC 1 SC1045
DATA READY
DATA READY RET.
THRESHOLD ADJ. (TEST POINT)
INHIBIT RET
MJ RET
CD RET
CORE MODULE SENSE / INHIBIT CIRCUITS
CHI
NOTES: (UNLESS OTHERWISE SPECIFIED)
1. REFER TO CD IC TABLE FOR IC NO & PIN CONNECTION
2. SYMBOL INDICATES INTERFACE BETWEEN CORE STACK AND CM-10. LETTER IN TRIANGULAR PORTION INDICATES STACK NUMBER IN RECTANGULAR PART IS WIRE NO., L TO R ON EDGE.
3. COMPONENT DES. DESIGNATION C3 NOT USED
4. RESISTOR VALUES ARE IN OHMS, ±5%, 1/8W
5. CAPACITORS VALUES ARE IN PF ±5%, 500V
6. FACTORY SELECTED VALUE, MAY NOT BE INSTALLED

FIGURE 31 4

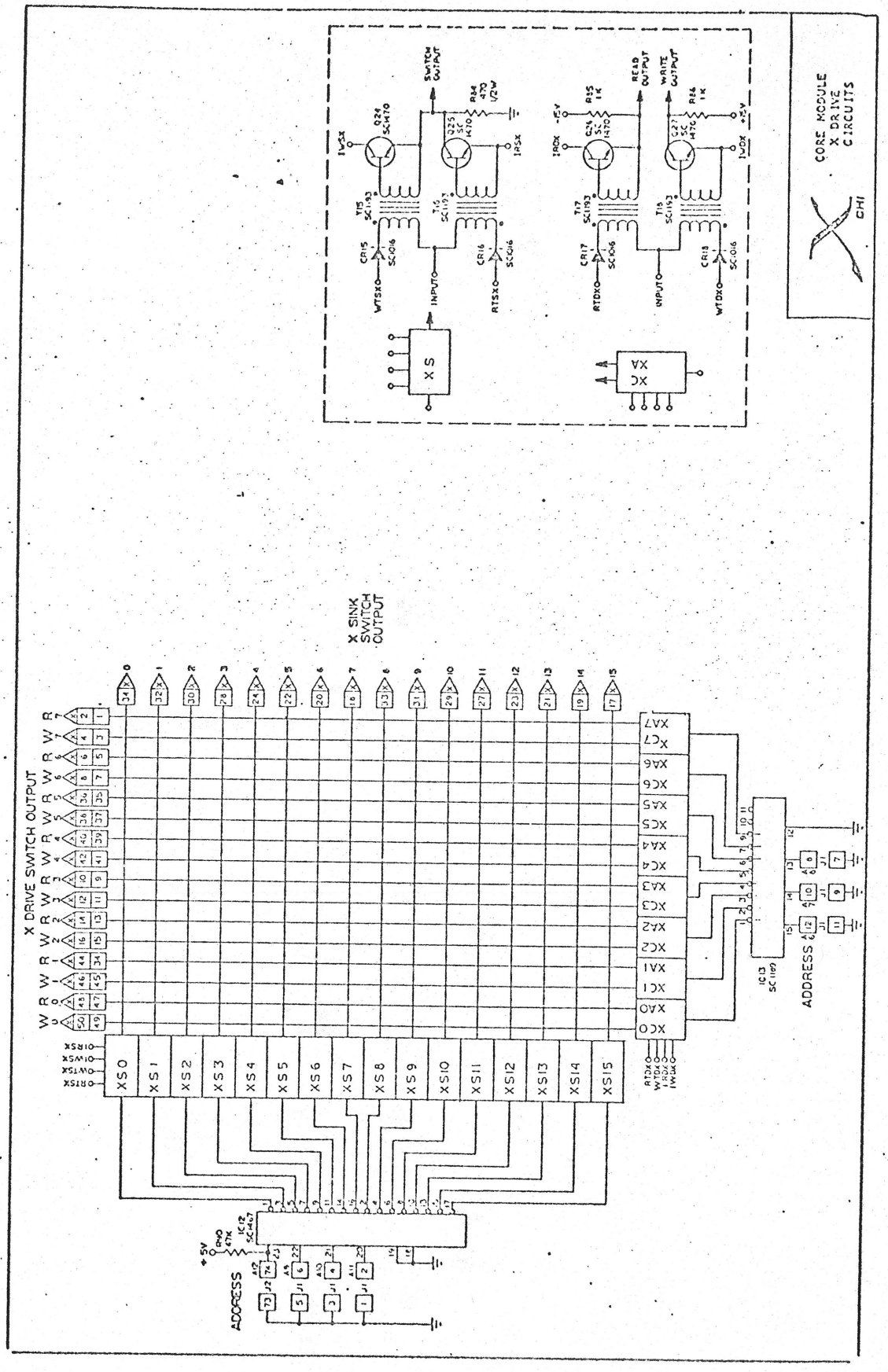

CORE MODULE
X DRIVE
CIRCUITS
CHI
SWITCH OUTPUT
READ OUTPUT
WRITE OUTPUT
INPUT0
X SINK
SWITCH
OUTPUT
X DRIVE SWITCH OUTPUT
ADDRESS
IC13
SC1189
IC12
SC1189
XS0
XS1
XS2
XS3
XS4
XS5
XS6
XS7
XS8
XS9
XS10
XS11
XS12
XS13
XS14
XS15

FIGURE 5

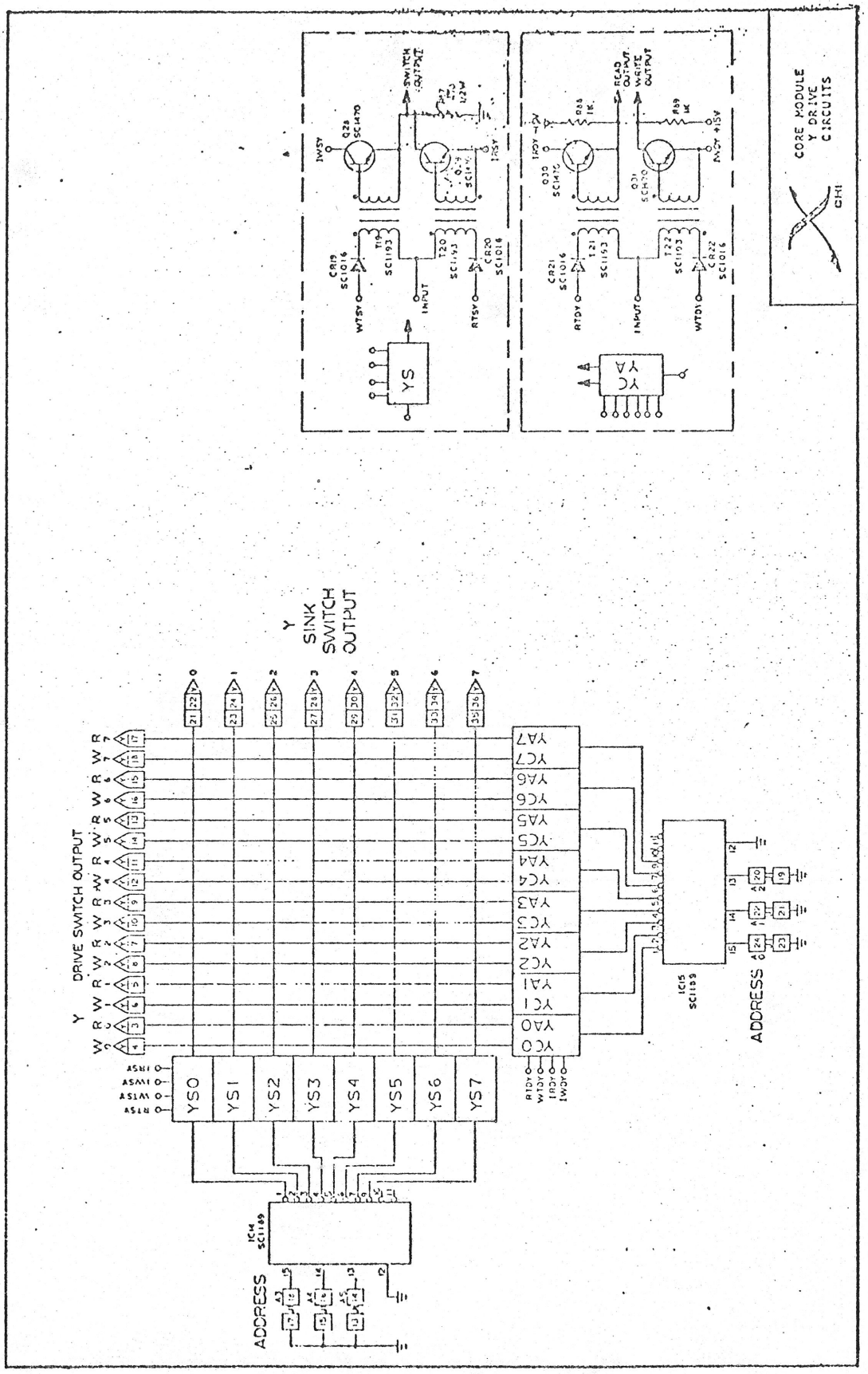
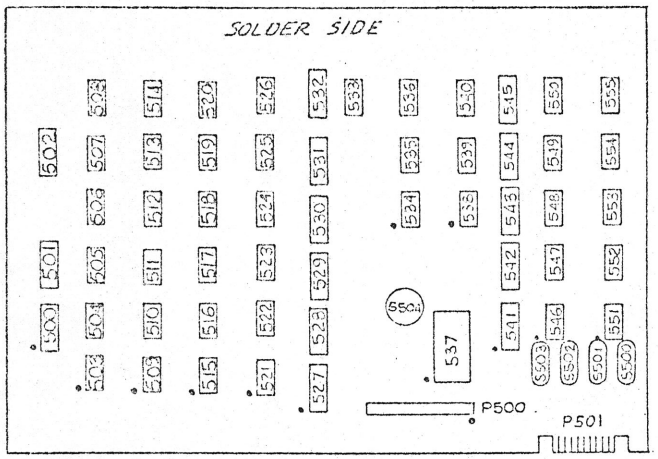

CORE MODULE
Y DRIVE
CIRCUITS
CH1
SWITCH OUTPUT
READ OUTPUT
WRITE OUTPUT
INPUT
YS
YC
YA
Y SINK SWITCH OUTPUT
Y DRIVE SWITCH OUTPUT
YS0
YS1
YS2
YS3
YS4
YS5
YS6
YS7
YA0
YA1
YA2
YA3
YA4
YA5
YA6
YA7
YC0
YC1
YC2
YC3
YC4
YC5
YC6
YC7
ADDRESS
ADDRESS

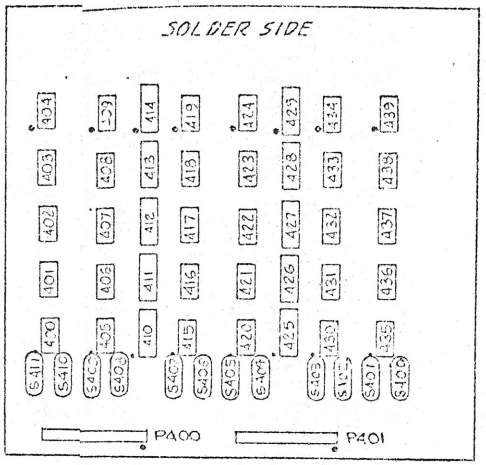
FIGURE 6

FRONT PANEL

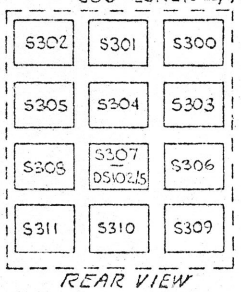
"500" BOARD (SH. 2,3,4 8,9,10 11 & 12)



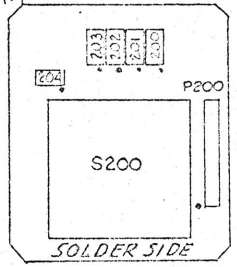
"400" BOARD (SH. 2,3,7,8,9,10 & 12)



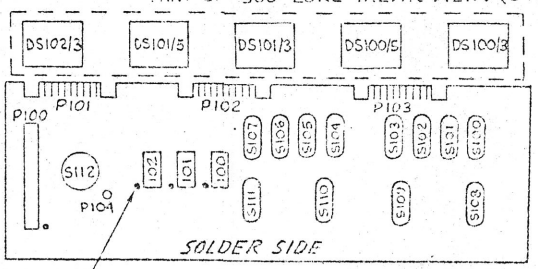
"300" ZONE (SH. 2,3,4 & 7)



"200" BOARD (SH. 2,3 & 6)



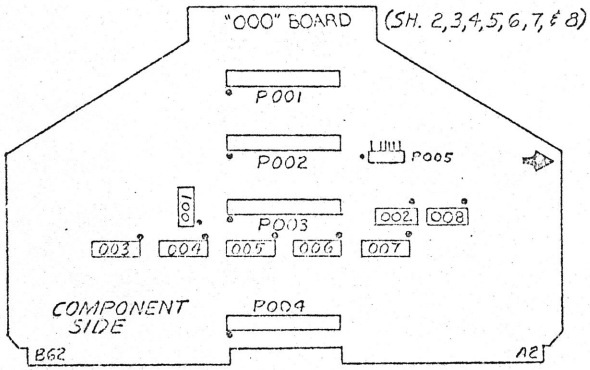
PART OF "300" ZONE (REAR VIEW) (SH. 2,3,4 & 7)

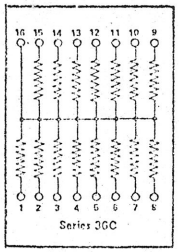


IC PIN 1 (TYP)

"100" BOARD (SH. 2,3,4,5 & 7)

"000" BOARD (SH. 2,3,4,5,6,7, & 8)

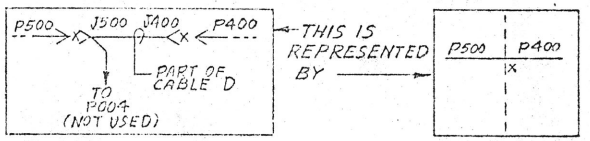




3.3K RESISTOR NETWORKS 001, 002

NOTES:

1. USED WITH PT. NUMBERS SHOWN ON SHEET 2.
2. LAMP REFERENCE DESIGNATIONS CONSIST OF DRIVER IC & PIN, E.G. DS 439/5, DS439/3, DS434/5, DS 434/3, ETC, FOR SHEET 9 THRU 12.
3. TITLES IN BOXES APPEAR ON FRONT PANEL OR ON PC FOIL AS APPLICABLE: ALL LAMP TITLES APPEAR ON FRONT PANEL.
4. ON SHEETS 9 THRU 12, SIGNALS CROSSING THE DASHED LINE DENOTE USAGE OF THAT PORTION OF CABLE D CONNECTING THE 400 & 500 BOARDS, IE:



WHERE X IS THE PIN, SOCKET, AND CONDUCTOR NUMBER.

5. DISTRIBUTION SYMBOLS (⏚, +5, VG, +LAMP, ETC) CONNECT TOGETHER ONLY THOSE CIRCUITS COMMON TO ANY ONE BOARD OR ZONE; CONNECTIONS BETWEEN BOARDS OR ZONES ARE SHOWN BY LINES.
6. DELETED
7. FOIL ARROW ON ALL PC BOARDS DESIGNATES COMPONENT SIDE OF BOARD. DIRECTION OF ARROW DESIGNATES TOP OF BOARD
8. -1 FRONT PANEL USES -1 "200" BOARD WITH DESCENDING KEY NUMBERS; -3 PANEL USES -3 BOARD WITH ASCENDING PATTERN.

QTY REQD	PART OR FILE NUMBER	NOMENCLATURE	MFG. PART NO. OR MATERIAL	MFG. NAME OR SPECIFICATION	ITEM NO
		LIST OF MATERIALS			

UNLESS OTHERWISE SPECIFIED
DIMENSION TOLERANCES
ANGULAR DIMENSION ± 1°
DECIMAL 2 PLACE ± .010
DECIMAL 3 PLACE ± .005
FRACTIONAL ±
BREAK SHARP EDGES MAX
INSIDE CORNERS MAX
ALL MACHINED SURFACES 63
CHAMFER ALL THREADS AT 45° TO THD. DIAMETER
DO NOT SCALE THIS PRINT

TITLE: PANEL, FRONT, 000 THRU 500 PORTION - 2130

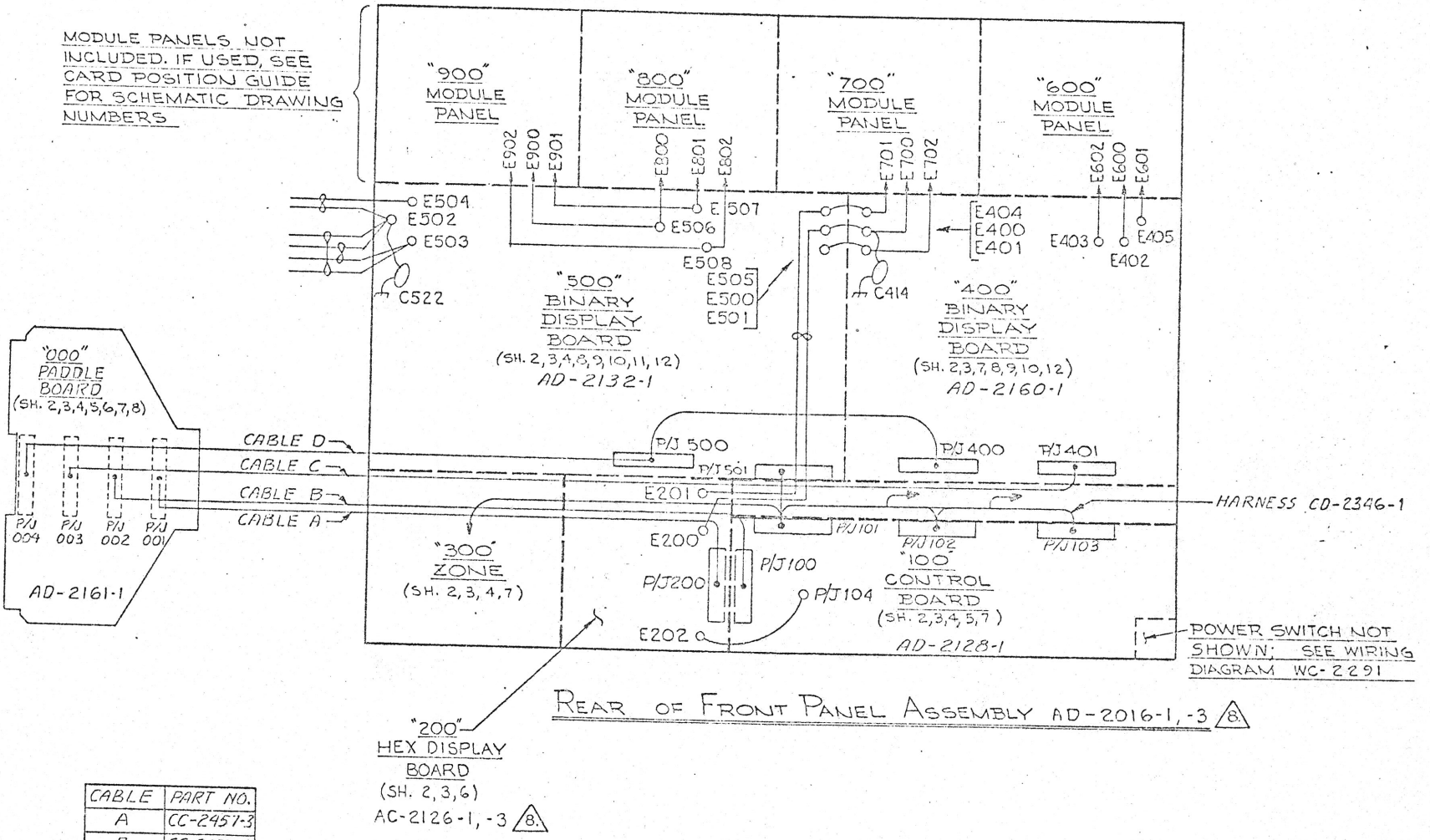
COMPUTER HARDWARE INC.

			DATE
DRAWN	KAE	6-18-74	
CHECKED	DOD	08-1-74	
DESIGN	THOMAS		
SCALE	NONE	APPROVED	SC

DWG. NO. 2111 SHEET 1 OF 15 REV. LET. C

LISTED	DWN	CHK	DATE
			2111

CHANGE RECORD NO

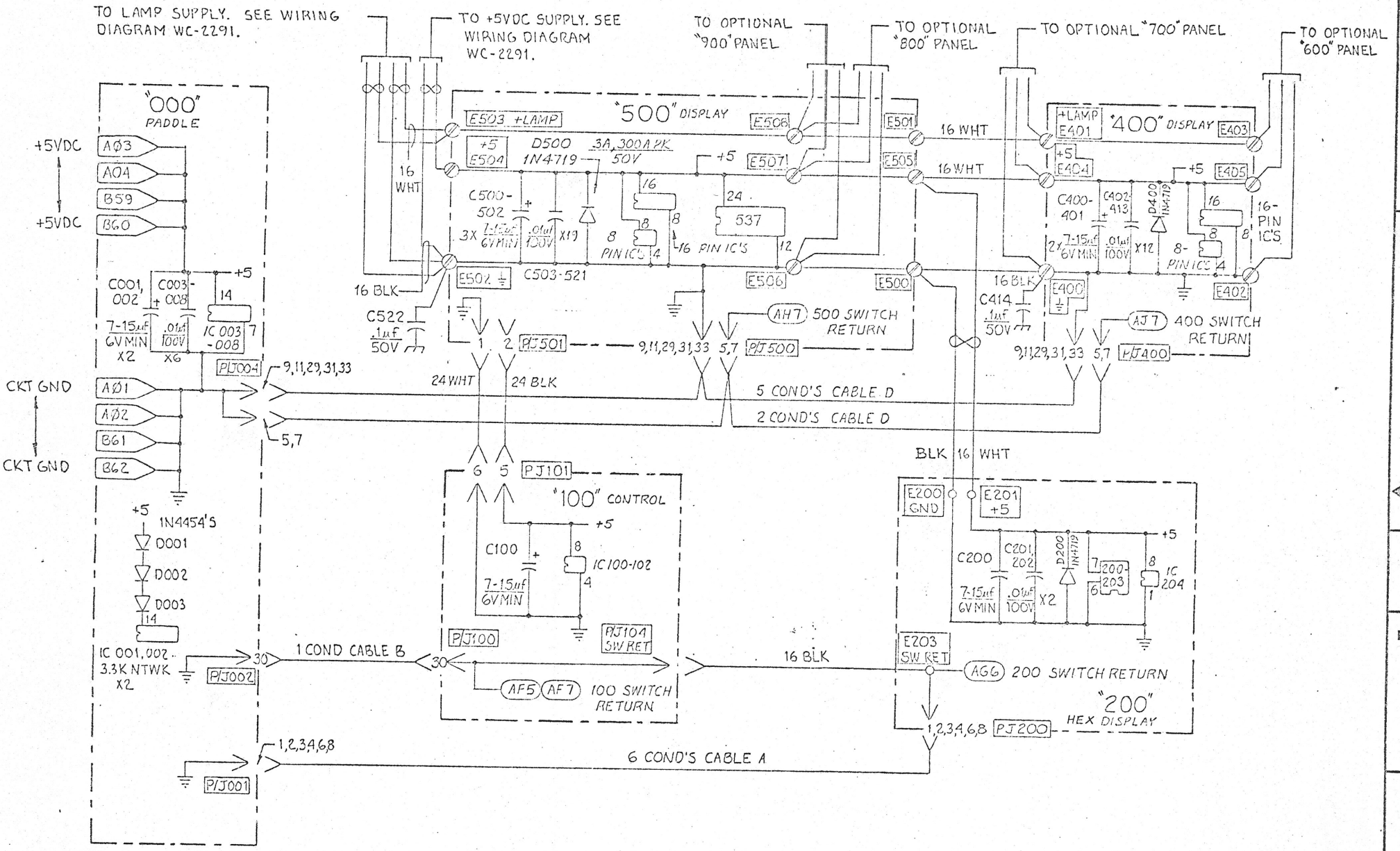


REAR OF FRONT PANEL ASSEMBLY AD-2016-1,-3 8.

CABLE	PART NO.
A	CC-2457-3
B	CC-2457-5
C	CC-2457-7
D	CC-2457-9

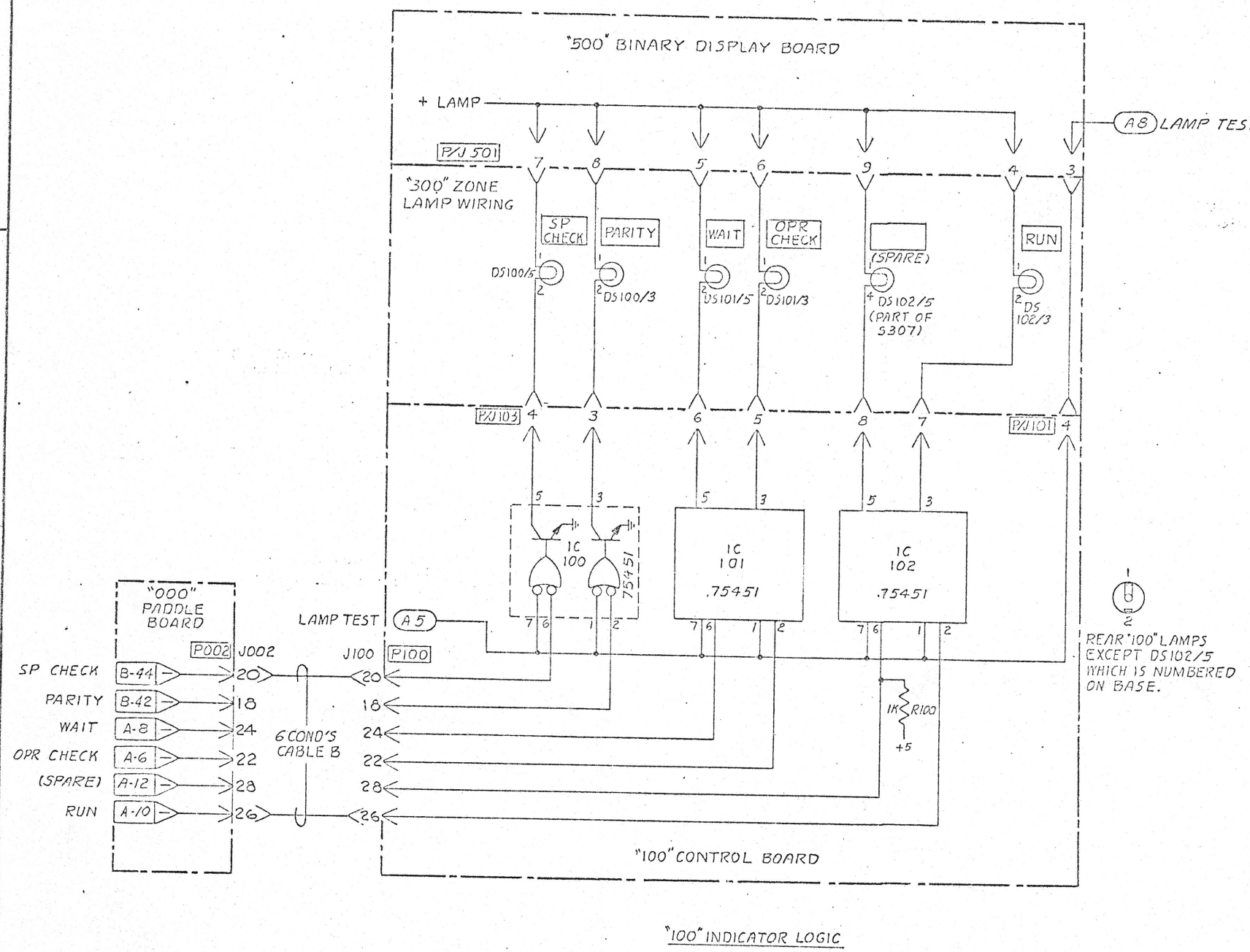
COMPUTER HARDWARE INC

SIZE SC | DWG NO 2111 | SHEET 2 OF 12 | REV C

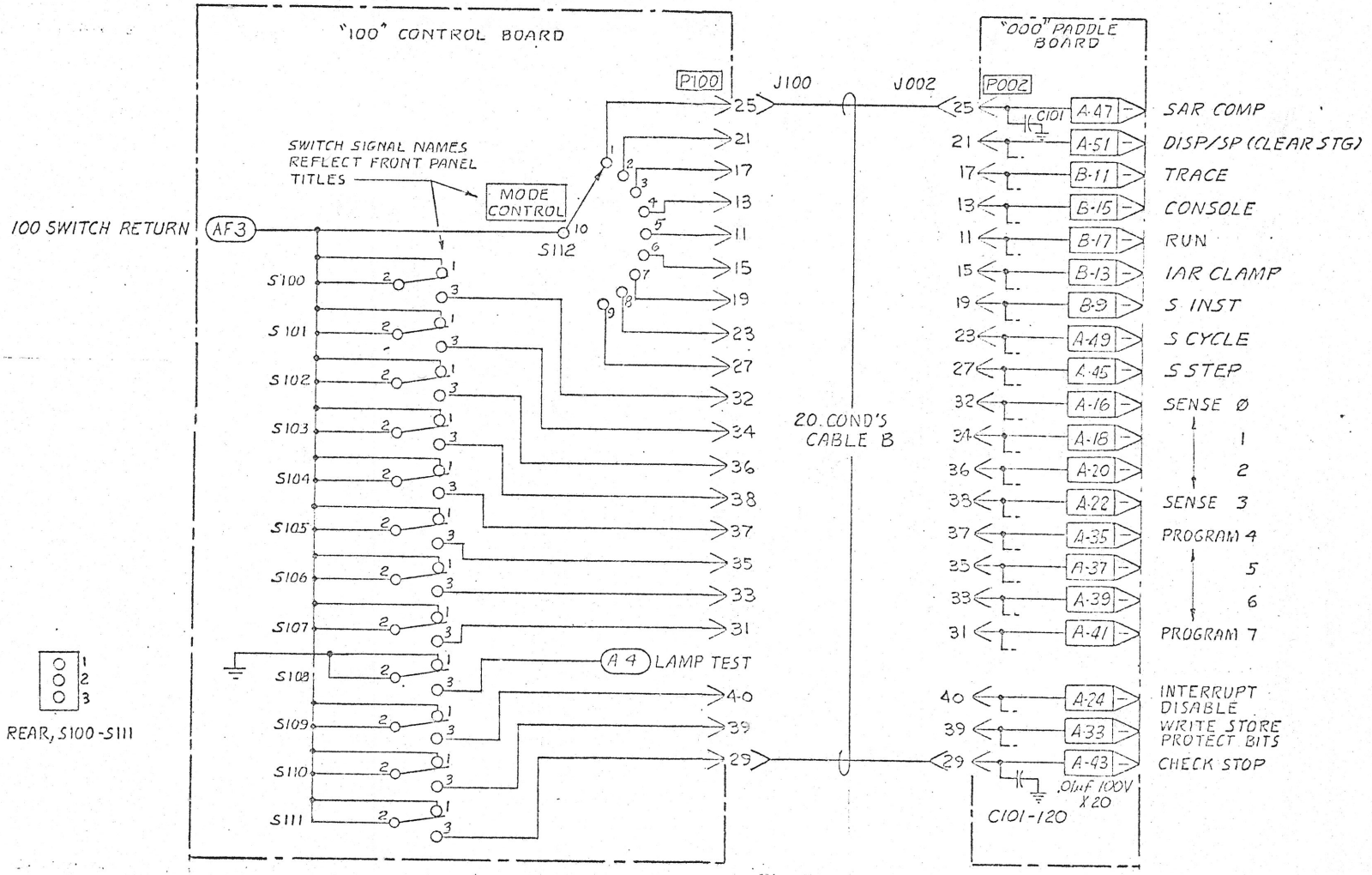


POWER DISTRIBUTION

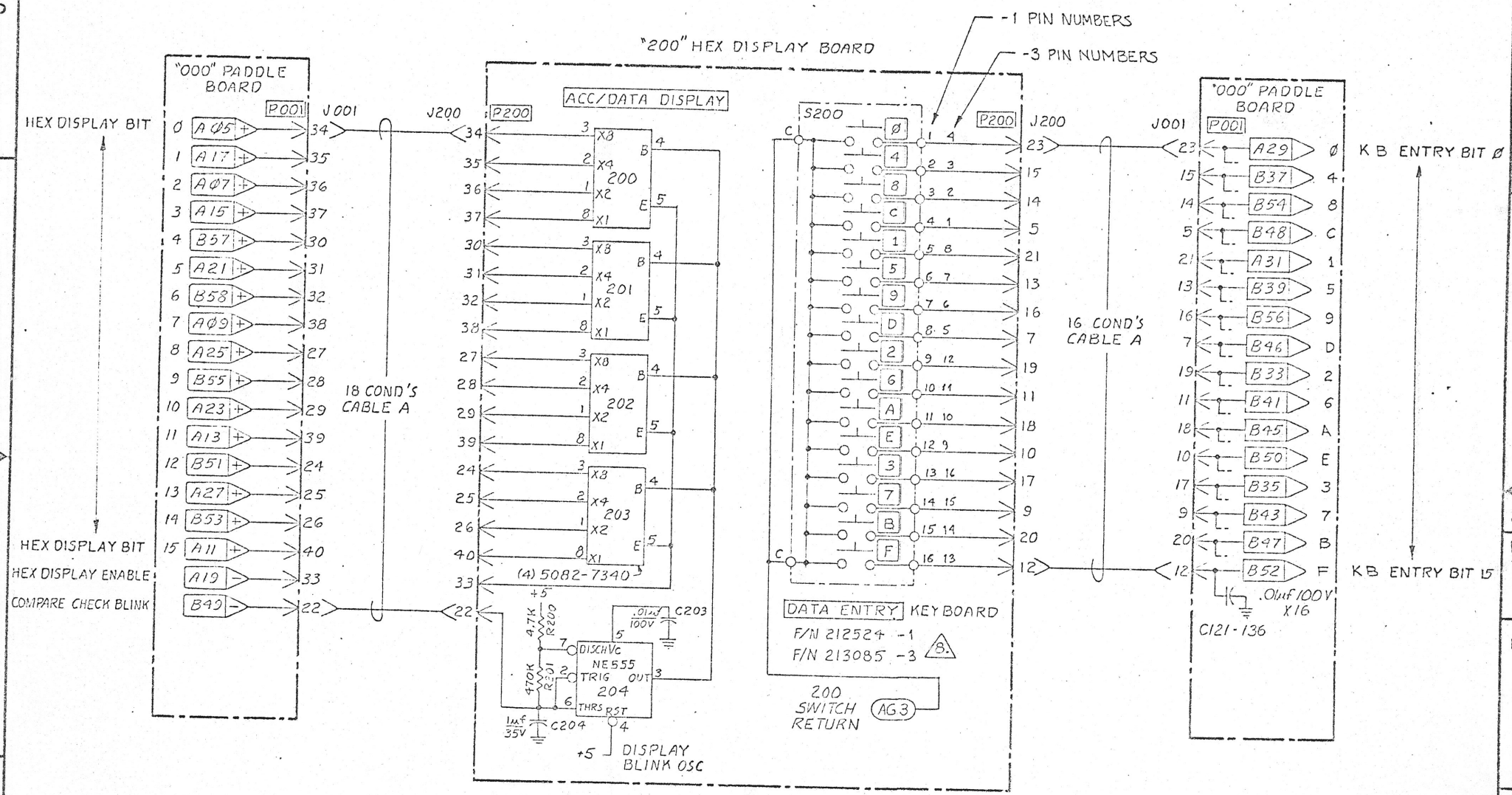
COMPUTER HARDWARE INC		
SC	2111 SHEET 3 OF 12	C



"100" INDICATOR LOGIC

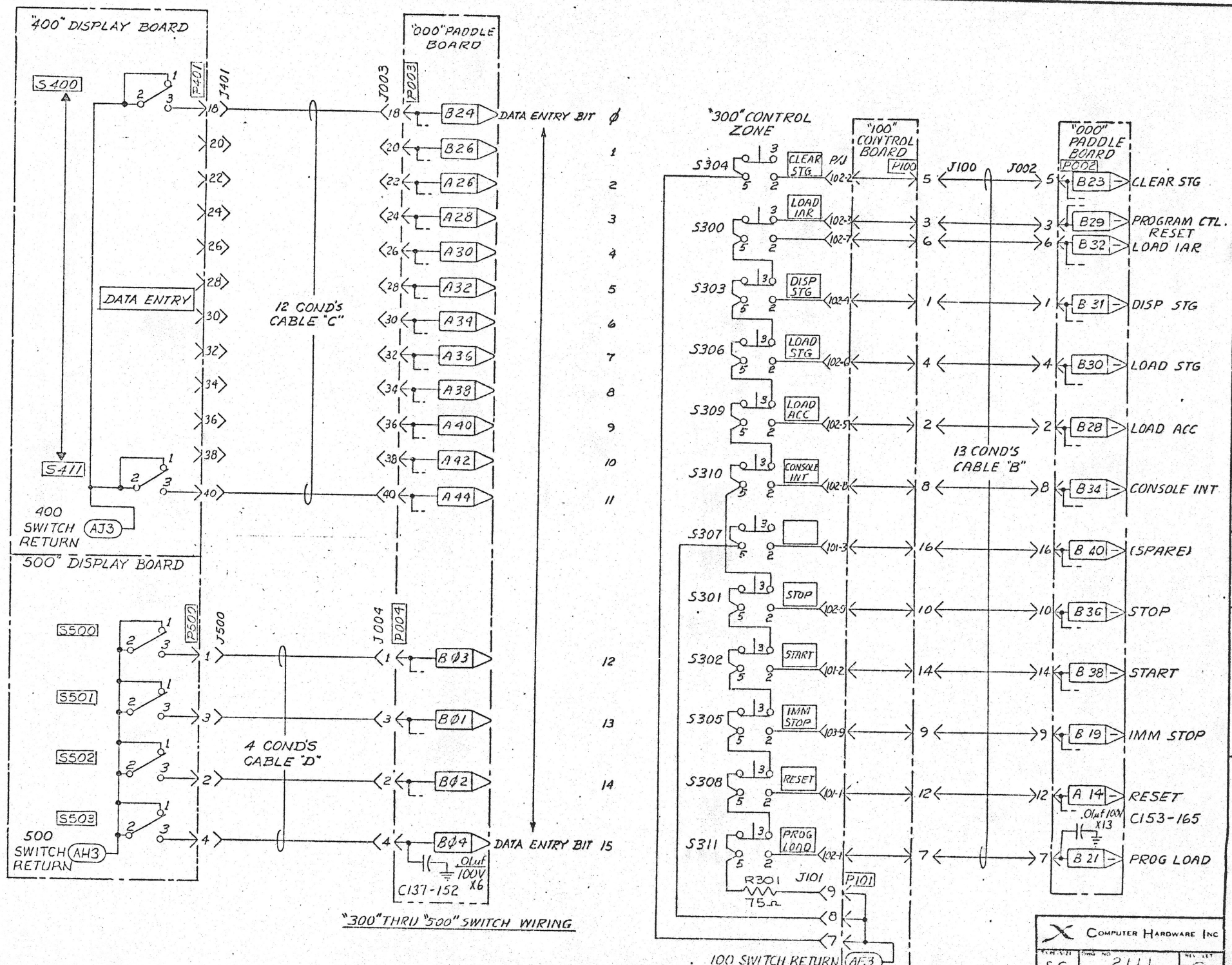


"100" CONTROL LOGIC

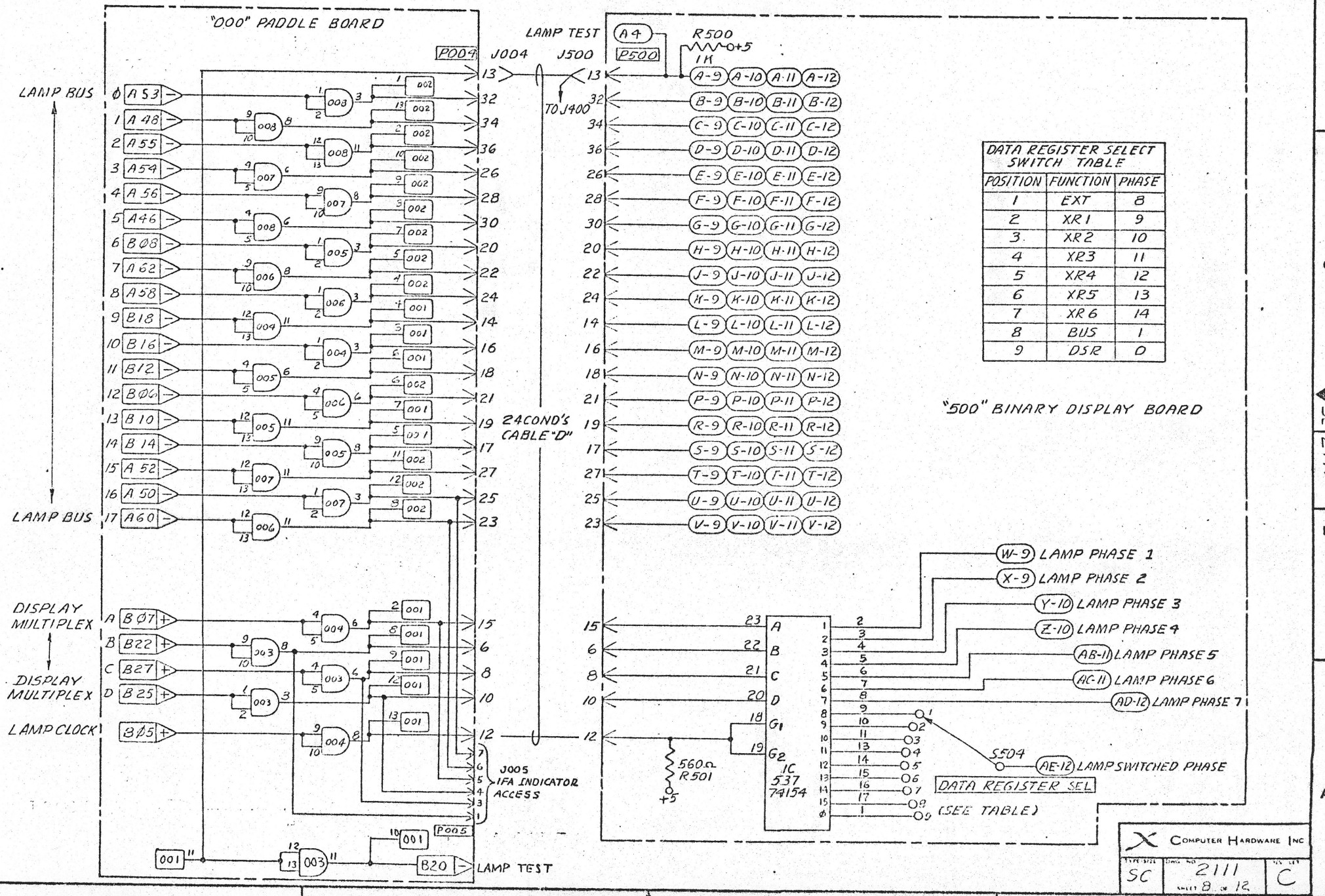


"200" HEX DISPLAY LOGIC

COMPUTER HARDWARE INC			
SYSTEM SC	DWG NO 2111 SHEET 5 OF 12	REV LET C	


"400" DISPLAY BOARD
"000" PADDLE BOARD
S400
P401
J401
P003
J003
DATA ENTRY
12 COND'S CABLE "C"
B24
DATA ENTRY BIT ϕ
B26
A26
A28
A30
A32
A34
A36
A38
A40
A42
A44
S411
400 SWITCH RETURN
AJ3
500" DISPLAY BOARD
S500
S501
S502
S503
P502
J500
J004
P004
4 COND'S CABLE "D"
BØ3
BØ1
BØ2
BØ4
DATA ENTRY BIT 15
.01uf 100V X6
C137-152
500 SWITCH RETURN
AH3
"300"THRU "500" SWITCH WIRING
"300" CONTROL ZONE
"100" CONTROL BOARD
"000" PADDLE BOARD
P100
J100
J002
P002
S304
CLEAR STG
P/J
102-2
B23
CLEAR STG
S300
LOAD IAR
102-3
102-7
B29
PROGRAM CTL. RESET
B32
LOAD IAR
S303
DISP STG
102-4
B31
DISP STG
S306
LOAD STG
102-6
B30
LOAD STG
S309
LOAD ACC
102-5
B28
LOAD ACC
13 COND'S CABLE "B"
S310
CONSOLE INT
102-8
B34
CONSOLE INT
S307
101-3
B 40
(SPARE)
S301
STOP
102-9
B36
STOP
S302
START
101-2
B 38
START
S305
IMM STOP
103-9
B 19
IMM STOP
S308
RESET
101-1
A 14
RESET
.01uf 100V X13
C153-165
S311
PROG LOAD
102-1
B 21
PROG LOAD
R301
75Ω
J101
P101
100 SWITCH RETURN
AF3
COMPUTER HARDWARE INC
SC
2111
SHEET 7 OF 12
C

"400" & "500" BINARY DISPLAY BOARD COMMON SIGNALS

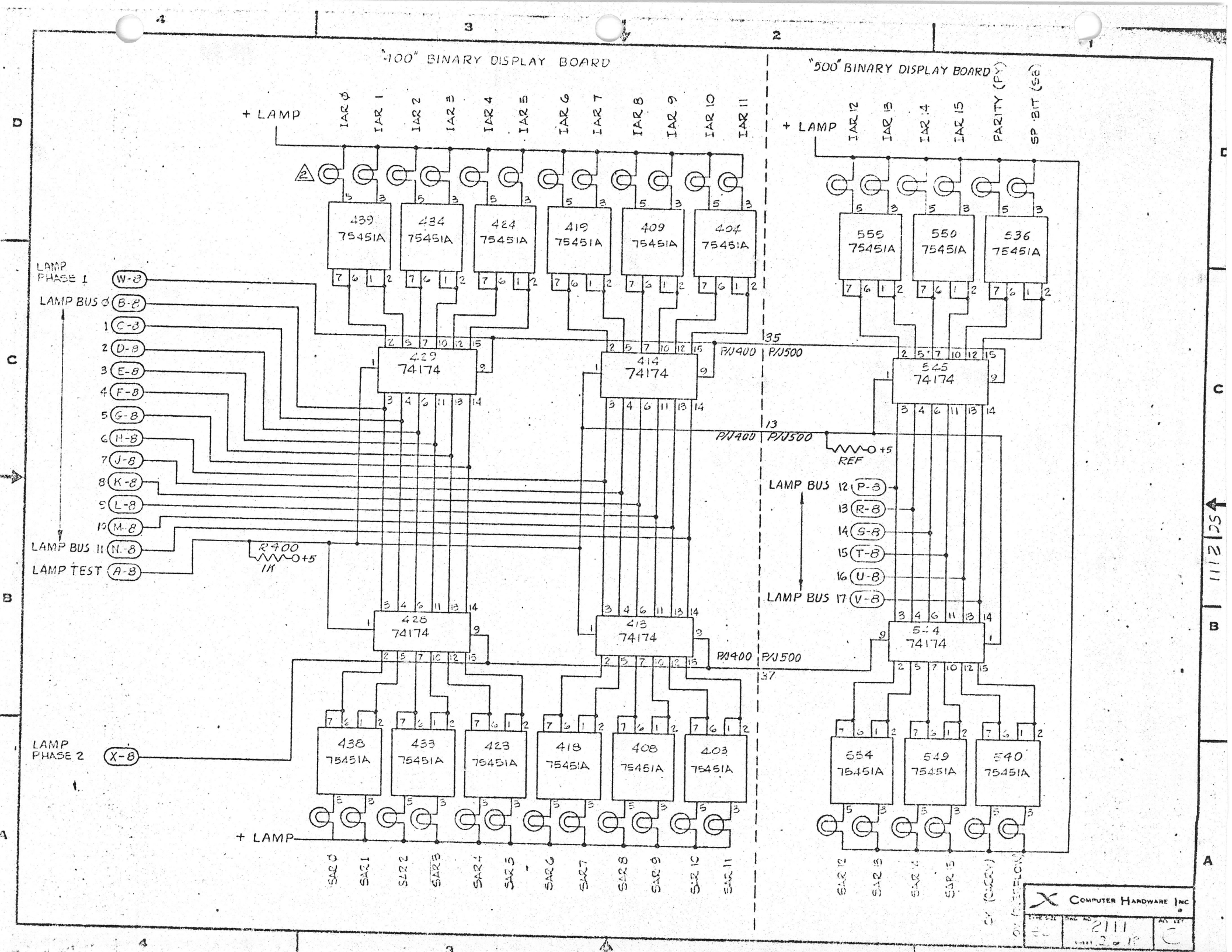


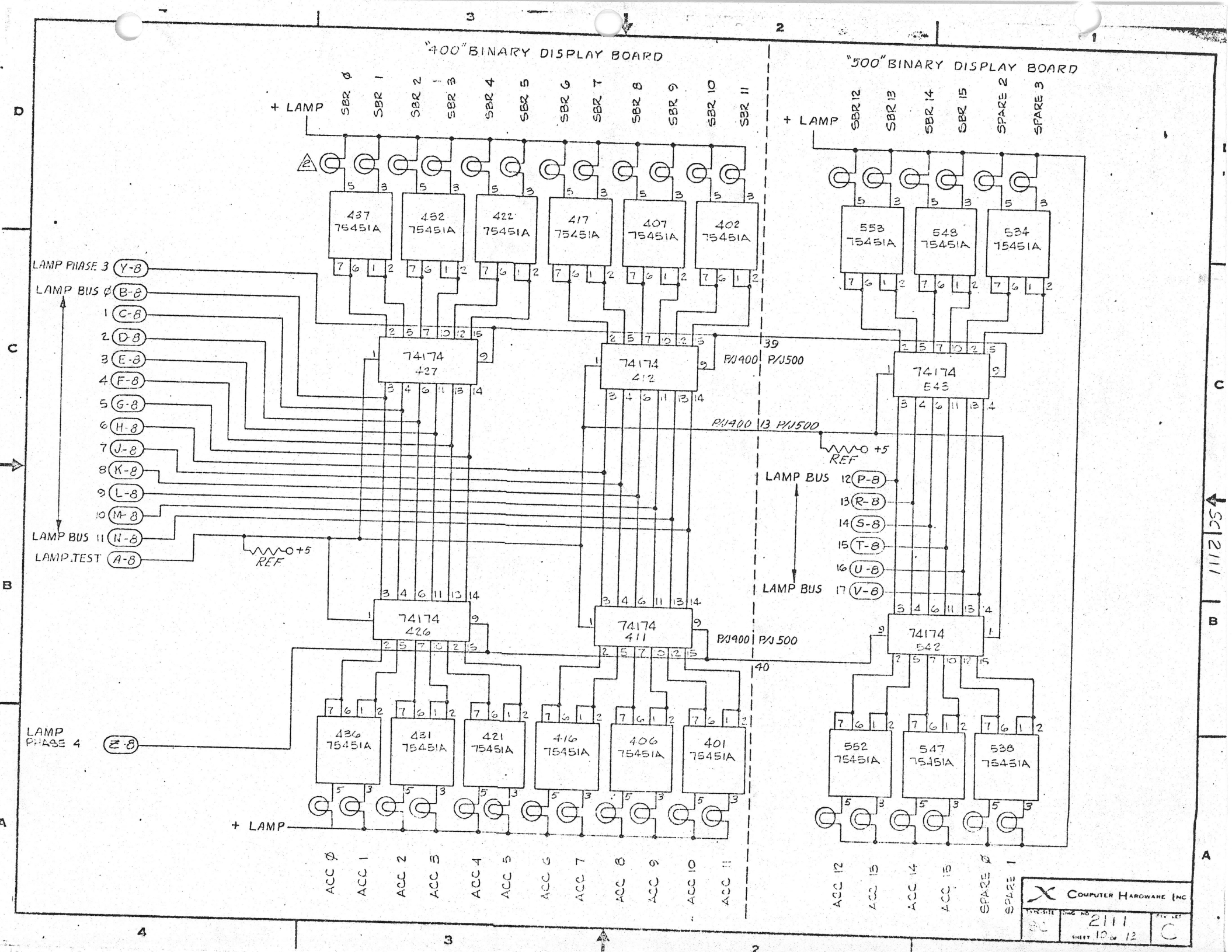
DATA REGISTER SELECT SWITCH TABLE		
POSITION	FUNCTION	PHASE
1	EXT	8
2	XR1	9
3	XR2	10
4	XR3	11
5	XR4	12
6	XR5	13
7	XR6	14
8	BUS	1
9	DSR	0

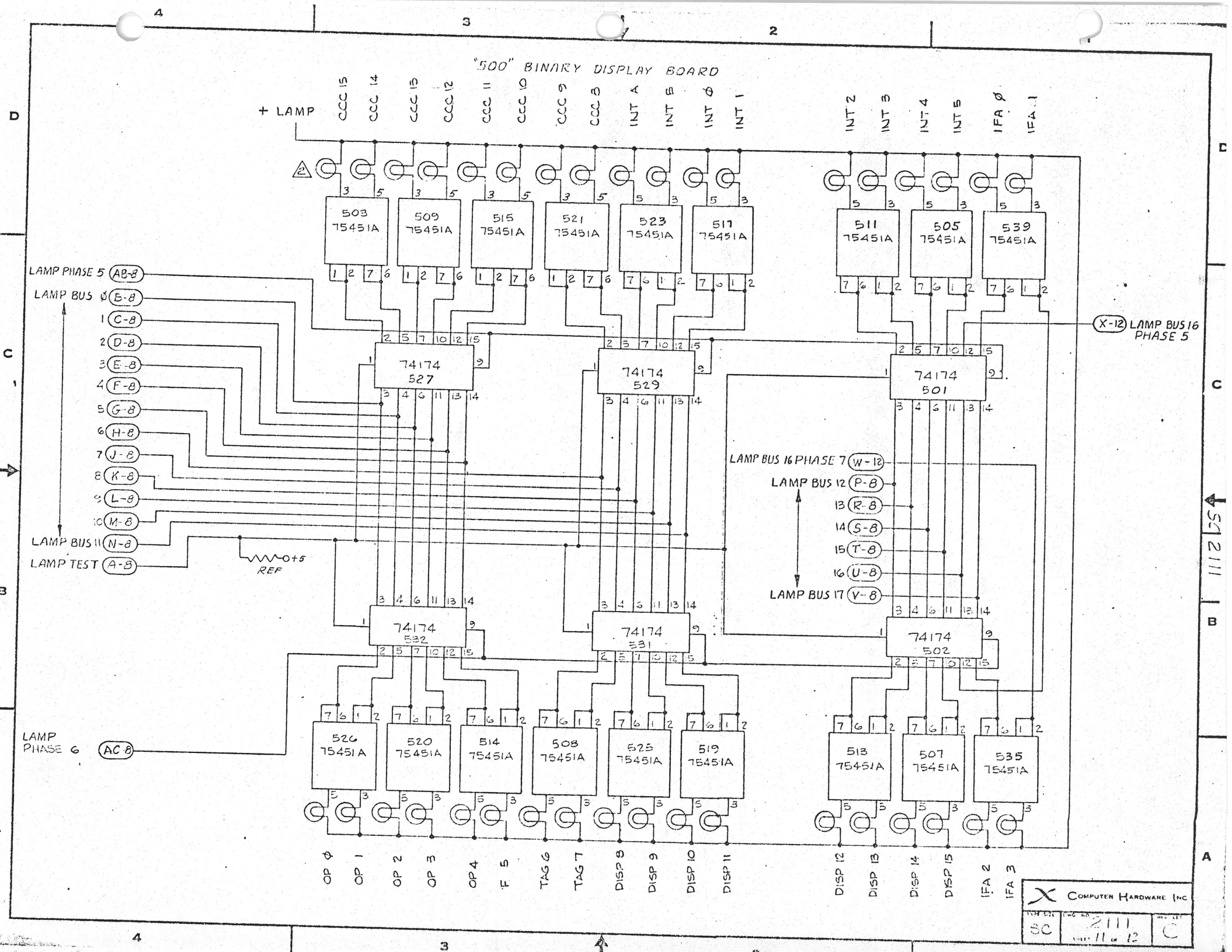
COMPUTER HARDWARE INC

SIZE	DWG NO	REV
SC	2111	C

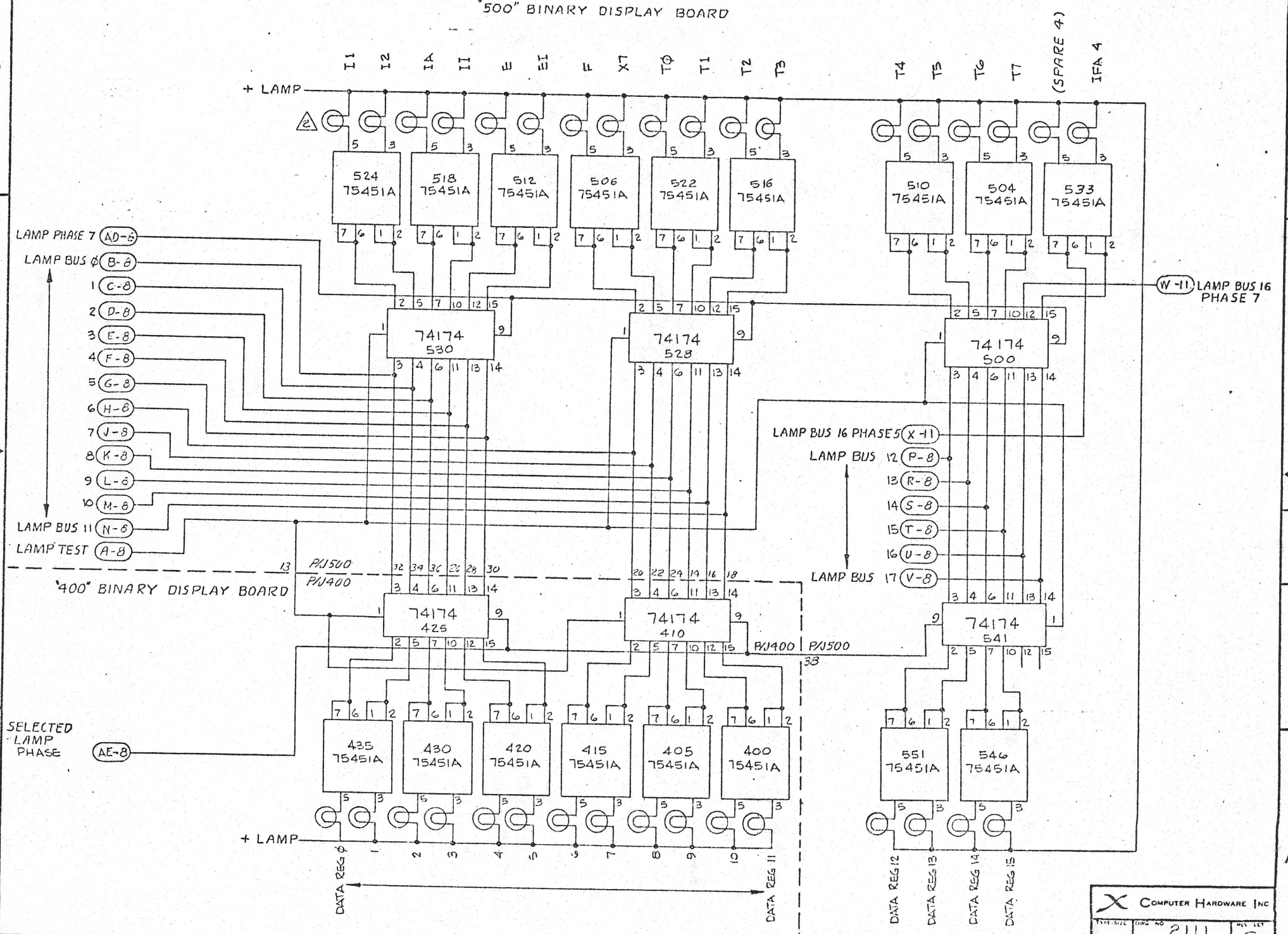
SHEET 8 OF 12


"400" BINARY DISPLAY BOARD
"500" BINARY DISPLAY BOARD
+ LAMP
IAR Ø
IAR 1
IAR 2
IAR 3
IAR 4
IAR 5
IAR 6
IAR 7
IAR 8
IAR 9
IAR 10
IAR 11
IAR 12
IAR 13
IAR 14
IAR 15
PARITY (PY)
SP BIT (SB)
439 75451A
434 75451A
424 75451A
419 75451A
409 75451A
404 75451A
555 75451A
550 75451A
536 75451A
LAMP PHASE 1
LAMP BUS Ø
LAMP BUS 11
LAMP TEST
W-8
B-8
C-8
D-8
E-8
F-8
G-8
H-8
J-8
K-8
L-8
M-8
N-8
A-8
R400
+5
429 74174
414 74174
545 74174
428 74174
413 74174
544 74174
P/J400
P/J500
35
13
37
REF
LAMP BUS
P-8
R-8
S-8
T-8
U-8
V-8
LAMP PHASE 2
X-8
438 75451A
433 75451A
423 75451A
418 75451A
408 75451A
403 75451A
554 75451A
549 75451A
540 75451A
SAR Ø
SAR 1
SAR 2
SAR 3
SAR 4
SAR 5
SAR 6
SAR 7
SAR 8
SAR 9
SAR 10
SAR 11
SAR 12
SAR 13
SAR 14
SAR 15
COMPUTER HARDWARE INC
2111


"400" BINARY DISPLAY BOARD
"500" BINARY DISPLAY BOARD
+ LAMP
SBR Ø
SBR 1
SBR 2
SBR 3
SBR 4
SBR 5
SBR 6
SBR 7
SBR 8
SBR 9
SBR 10
SBR 11
SBR 12
SBR 13
SBR 14
SBR 15
SPARE 2
SPARE 3
437 75451A
432 75451A
422 75451A
417 75451A
407 75451A
402 75451A
553 75451A
548 75451A
534 75451A
LAMP PHASE 3 Y-8
LAMP BUS Ø B-8
1 C-8
2 D-8
3 E-8
4 F-8
5 G-8
6 H-8
7 J-8
8 K-8
9 L-8
10 M-8
LAMP BUS 11 N-8
LAMP TEST A-8
74174 427
74174 412
74174 543
P/J400
P/J500
39
13
+5 REF
LAMP BUS 12 P-8
13 R-8
14 S-8
15 T-8
16 U-8
LAMP BUS 17 V-8
74174 426
74174 411
74174 542
40
LAMP PHASE 4 Z-8
436 75451A
431 75451A
421 75451A
416 75451A
406 75451A
401 75451A
562 75451A
547 75451A
538 75451A
ACC Ø
ACC 1
ACC 2
ACC 3
ACC 4
ACC 5
ACC 6
ACC 7
ACC 8
ACC 9
ACC 10
ACC 11
ACC 12
ACC 13
ACC 14
ACC 15
SPARE Ø
SPARE 1
COMPUTER HARDWARE INC
SIZE C
DWG NO 2111
SHEET 10 OF 12
REV LET C

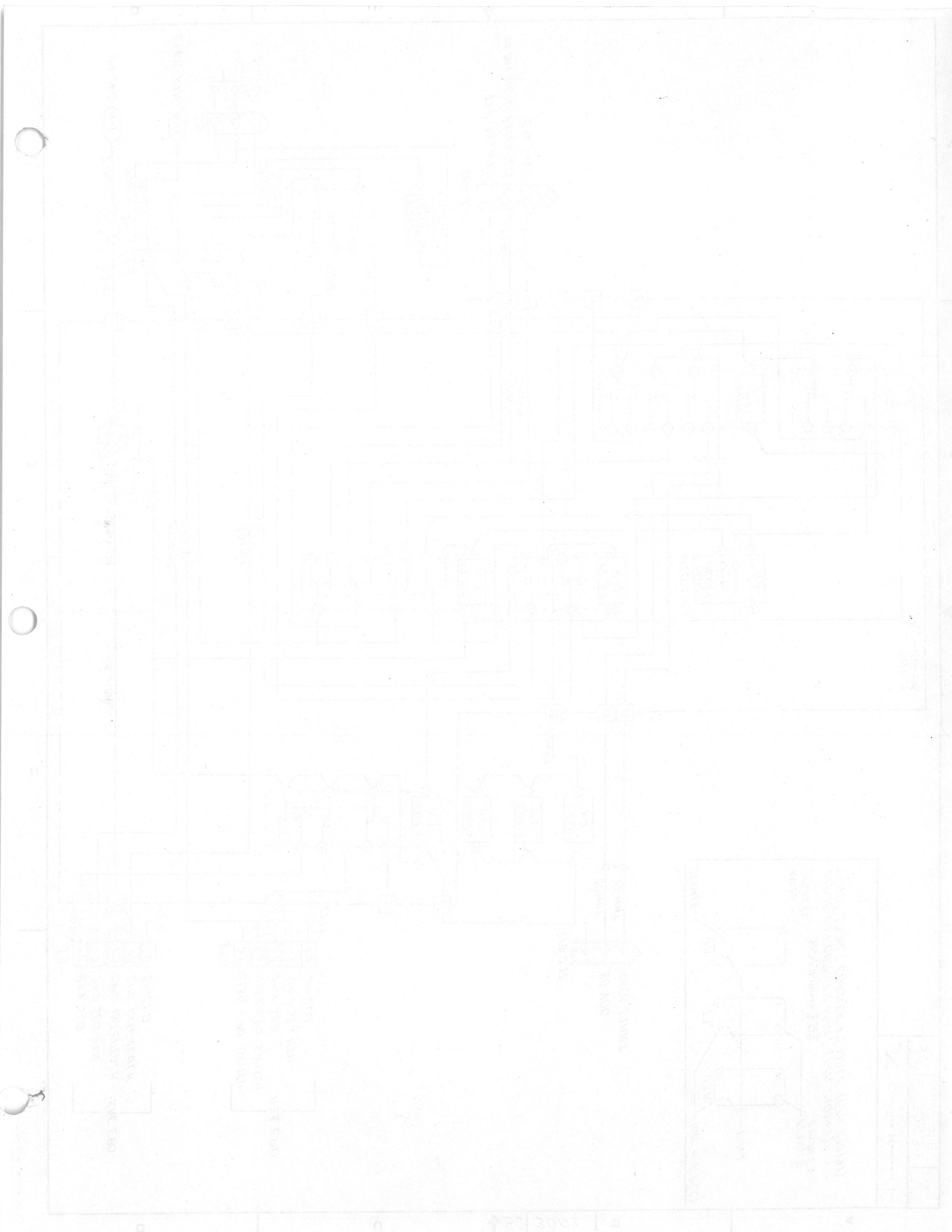

"500" BINARY DISPLAY BOARD
+ LAMP
CCC 15
CCC 14
CCC 13
CCC 12
CCC 11
CCC 10
CCC 9
CCC 8
INT A
INT B
INT C
INT 1
INT 2
INT 3
INT 4
INT 5
IFA 0
IFA 1
503 75451A
509 75451A
515 75451A
521 75451A
523 75451A
517 75451A
511 75451A
505 75451A
539 75451A
LAMP PHASE 5 AB-8
LAMP BUS 0 B-8
1 C-8
2 D-8
3 E-8
4 F-8
5 G-8
6 H-8
7 J-8
8 K-8
9 L-8
10 M-8
LAMP BUS 11 N-8
LAMP TEST A-8
+5 REF
74174 527
74174 529
74174 501
74174 532
74174 531
74174 502
X-12 LAMP BUS 16 PHASE 5
LAMP BUS 16 PHASE 7 W-12
LAMP BUS 12 P-8
13 R-8
14 S-8
15 T-8
16 U-8
LAMP BUS 17 V-8
LAMP PHASE 6 AC-8
526 75451A
520 75451A
514 75451A
508 75451A
525 75451A
519 75451A
518 75451A
507 75451A
535 75451A
OP 0
OP 1
OP 2
OP 3
OP 4
F 5
TAG 6
TAG 7
DISP 8
DISP 9
DISP 10
DISP 11
DISP 12
DISP 13
DISP 14
DISP 15
IFA 2
IFA 3
COMPUTER HARDWARE INC
SC
2111
11 of 12
C

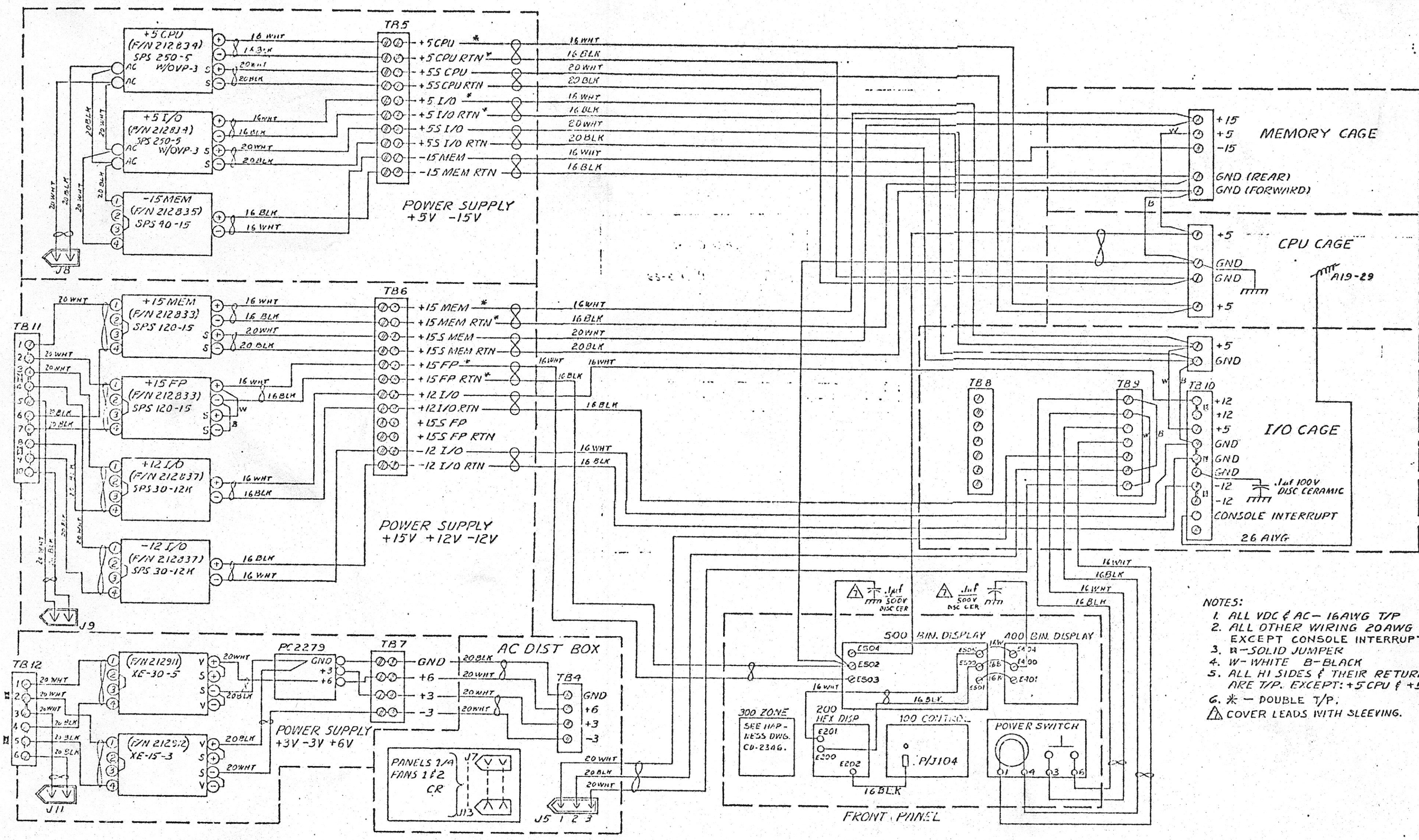
"500" BINARY DISPLAY BOARD



COMPUTER HARDWARE INC			
SIZE 5C	DWG NO 2111	SHEET 12 OF 12	REV LET C

AC & DC POWER DISTRIBUTION





NOTES:
1. ALL VDC & AC – 16AWG T/P
2. ALL OTHER WIRING 20AWG T/P EXCEPT CONSOLE INTERRUPT (26 AWG)
3. B – SOLID JUMPER
4. W – WHITE B – BLACK
5. ALL HI SIDES & THEIR RETURNS ARE T/P. EXCEPT: +5 CPU & +5 CPU RTN.
6. ✳ – DOUBLE T/P.
7. △ COVER LEADS WITH SLEEVING.

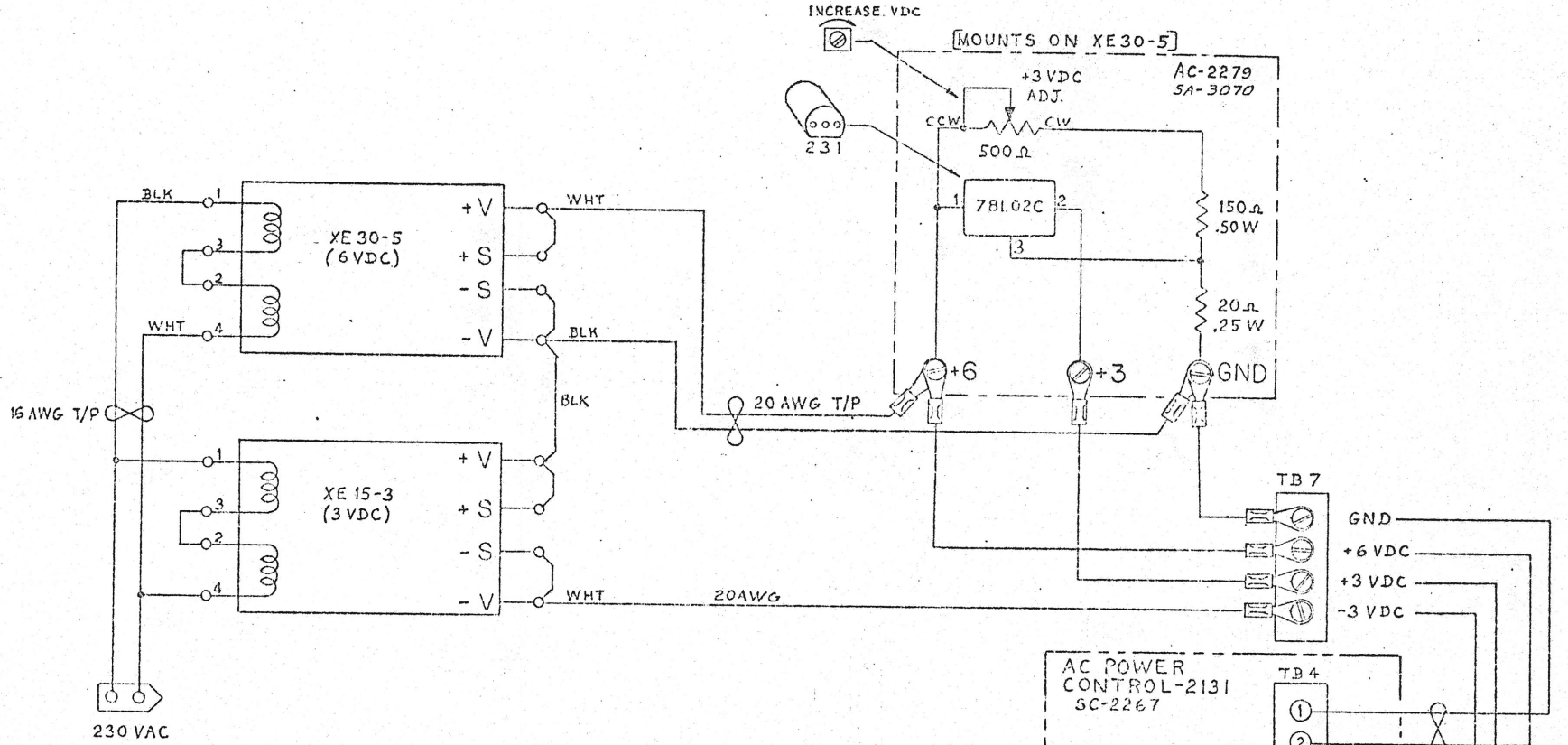
MOLEX CONNECTORS

POWER WIRING - 2131

Computer Hardware Inc.

WD 2291 B

NOTES:
1. THIS DRAWING USED IN CONJUNCTION WITH AC-2350.



CONFIGURATION TABLE										
SA-3070	NC									
RC-2279	NC									
NC-2279	NC									

PART OR EILE NUMBER	NOMENCLATURE	MFG. PART NO. OR MATERIAL	MFG. NAME OR SPECIFICATION	ITEM NO.	QTY. REQ'D

LIST OF MATERIALS

THIS PRINT CONTAINS PROPRIETARY INFORMATION. REPRODUCTION OF THIS PRINT OR ANY INFORMATION CONTAINED HEREON OR MANUFACTURE OF ANY ARTICLES SHOWN HEREON, DISCLOSURE TO OTHERS IS FORBIDDEN EXCEPT BY SPECIFIC WRITTEN PERMISSION FROM COMPUTER HARDWARE, INC.

UNLESS OTHERWISE SPECIFIED
DIMENSION TOLERANCES
ANGULAR DIMENSION ± 0°
DECIMAL 2 PLACE ± .010
DECIMAL 3 PLACE ± .005
FRACTIONAL ±
BREAK SHARP EDGES MAX
FINISH CORNERS MAX
ALL MACHINE SURFACES
CHAMFER ALL THREADS
DO NOT SCALE THIS PRINT

TITLE: POWER SUPPLY, DC, 1442-2131

COMPUTER HARDWARE INC.
25 SEP 74

DRAWN: D. WOODSON
CHECKED:
DESIGN: L.C.W.
SCALE:
TYPE/SIZE: SC
DWG NO: 2277
SHEET 1 OF 1
REV LTR: NC2

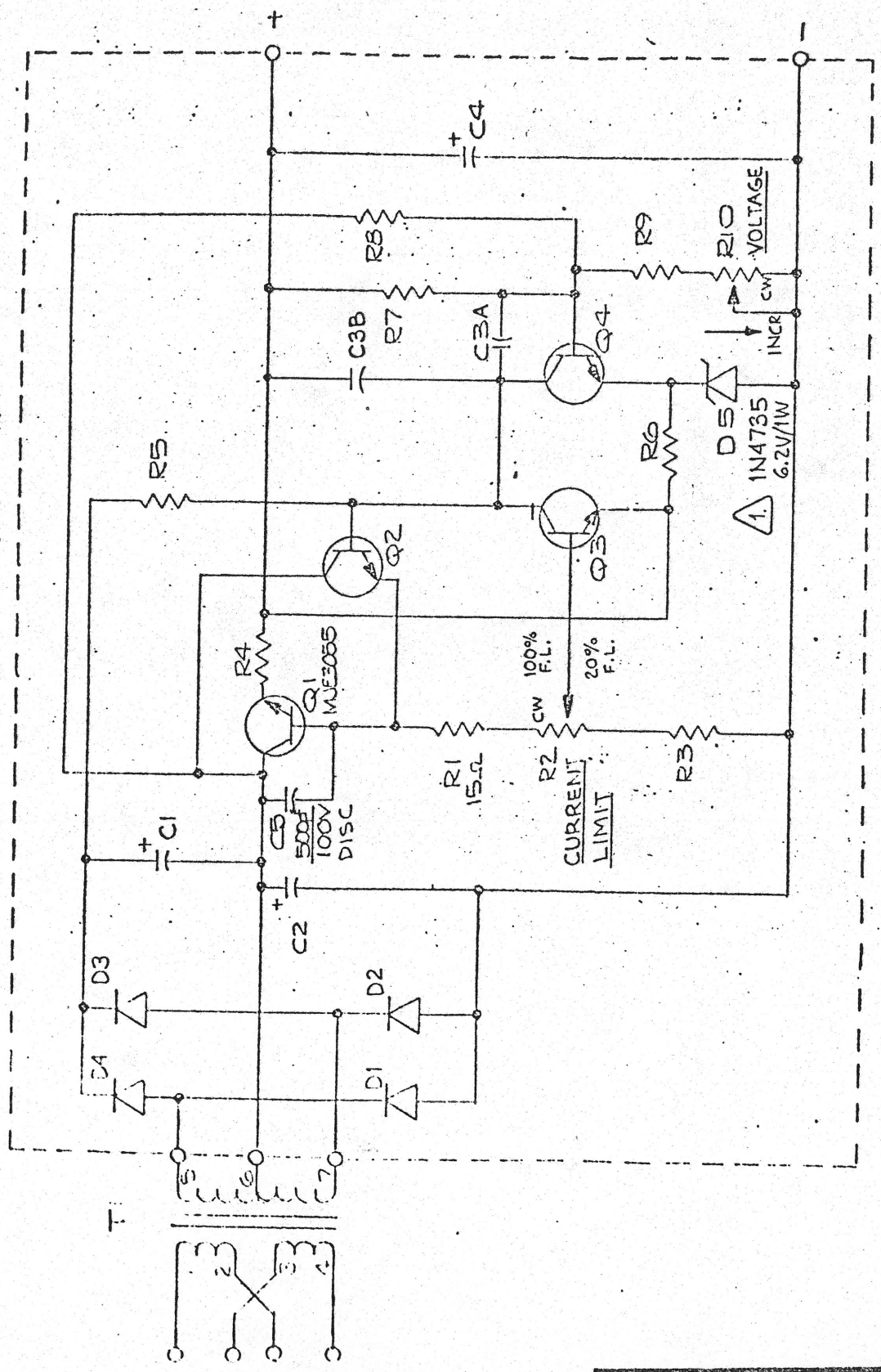
CHANGE ENGINEERING 2277

SC 22771 B

TITLE

POWER SUPPLIES, NOMINAL 12-48VDC, 15-30W
STANDARD POWER INC. SPS 15/30

COMPUTER HARDWARE INC.



RECTIFIER RATINGS (SEE SHEET 2)			
1N5391	50V	1.5A	
1N5392	100V	1.5A	
1N5401	100V	3.0A	
1N5402	200V	3.0A	

TYPE-SIZE	DWG NO.	REV LET.
SA	1826 SHEET 1 OF 2	NC

TITLE

POWER SUPPLIES, NOMINAL 12-48VDC, 15-30W,
STANDARD POWER INC. SPS 15/30

COMPUTER HARDWARE INC

TABLE OF UNIQUE COMPONENTS

PART	15-12	30-12	15-15	30-15	15-24/28	30-24/28	30-48
C1	50UF/50V						50UF/75V
C2	1100UF/30V	2900UF/30V	1100UF/30V	2900UF/30V	650UF/50V	1700UF/50V	600UF/100V
C3A	.01UF/100V				500PF/100V		—
C3B	—	—	—	—	—	—	.01UF/100V
C4	250UF/15V			200UF/20V		50UF/50V	50UF/75V
D1,D2	1N5391					1N5401	1N5402
D3, D4	1N5391						1N5392
Q2	2N3404						D33D29
Q3,Q4	2N3416						D33D29
R2	100Ω/2W					250Ω/2W	500Ω/2W
R3	1.2K		1.5K	1.2K	5.6K		10K
R4	.33Ω/2W		.56Ω/2W	.33Ω/2W	1.2Ω/2W	.56Ω/2W	1Ω/2W
R5	6.2K				1.2K	12K	43K
R6	1K				2.7K		5.1K
R7 (VALUES FOR D5 VOLTAGE)	200Ω 5.9-6.09V		330Ω 5.9-6.09V		2K±1% 6.0-6.09V		8.06K±2%
	180Ω 6.1-6.29V		300Ω 6.1-6.29V		1.91K±1% 6.1-6.19V		
			270Ω 6.3-6.49V		1.87K±1% 6.2-6.29V		
R8	820K						1.5M
R9	200Ω±2%			560Ω±2%			1.13K±2%
R10	100Ω/2W				250Ω/2W		500Ω/2W
T1 P/N	101148	101021	101176	101077	101172	101022	101092

NOTES:

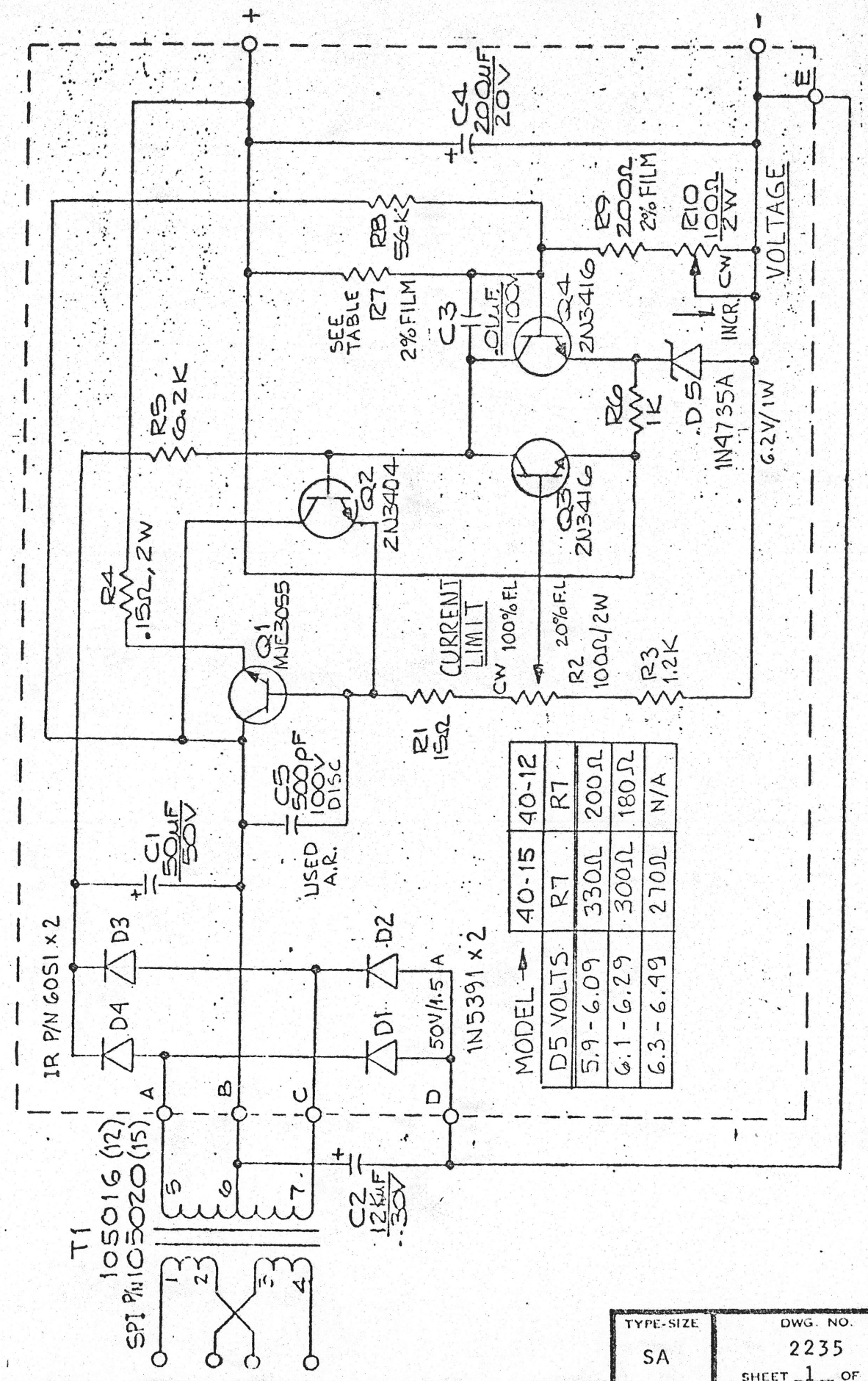
1. ON P/N SPS-30-48, D5 IS SELECTED TO 5.9-6.49V.
2. RESISTORS ARE 1/2W UNLESS NOTED
3. SUFFIX "K" TO PART NUMBER DENOTES POWER SUPPLY COMPONENTS ARE FASTENED WITH SCREWS (VS. RIVETS).

TYPE-SIZE	DWG. NO.	REV.
SA	1826 SHEET 2 OF 2	

TITLE

POWER SUPPLIES, 10.8-12.9 & 13.2-16.5VDC 40W, STANDARD POWER INC., SPS 40-12,-15

COMPUTER HARDWARE INC.



MODEL →	40-15	40-12
D5 VOLTS	R7	R7
5.9 - 6.09	330Ω	200Ω
6.1 - 6.29	300Ω	180Ω
6.3 - 6.49	270Ω	N/A

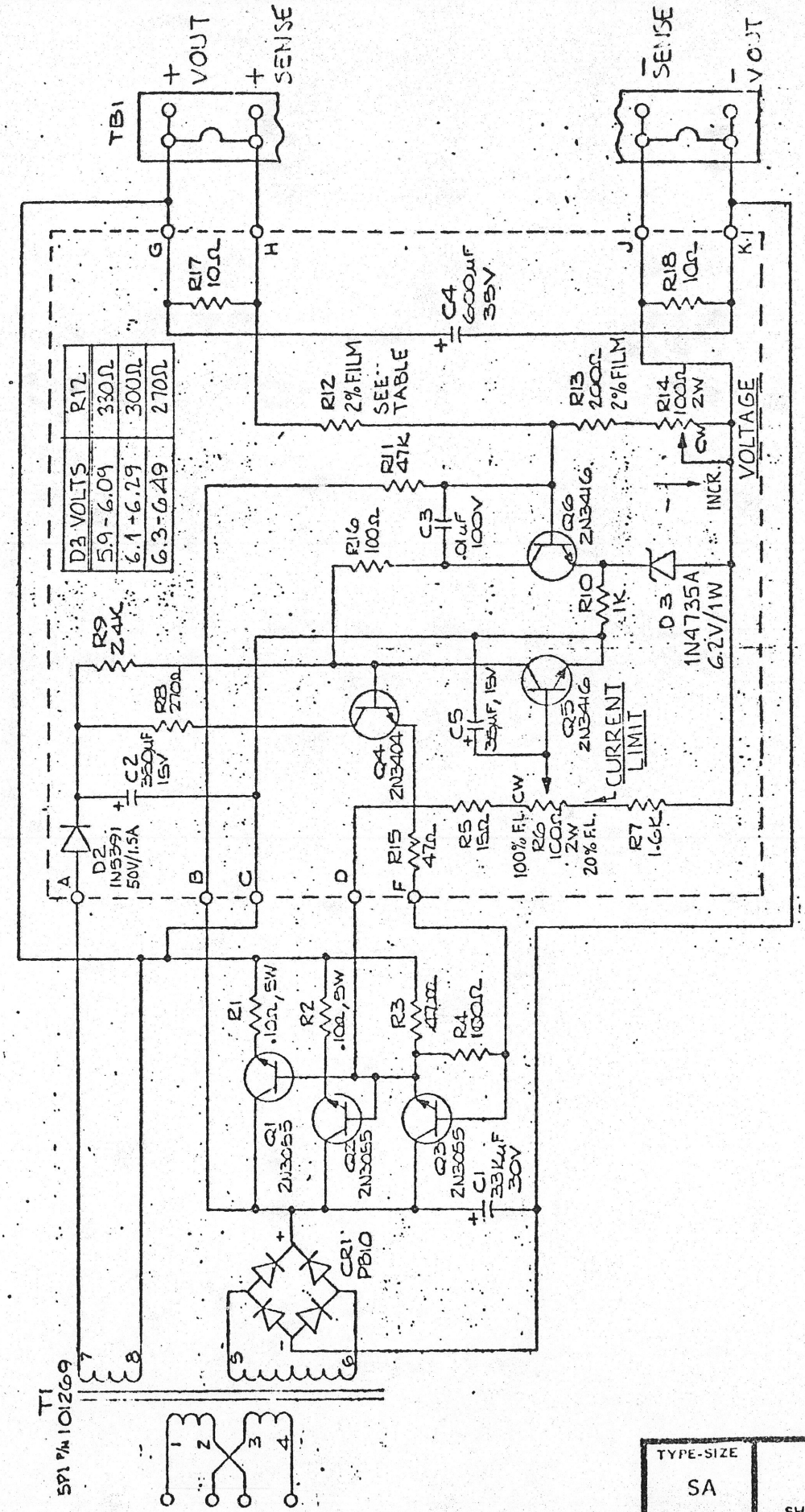
NOTE:
1. ALL RESISTORS 1/2 W. UNLESS NOTED.

TYPE-SIZE	DWG. NO.	REV. LET.
SA	2235	NC
	SHEET 1 OF 1	

TITLE

POWER SUPPLY, 14-18VDC, 120W, STANDARD POWER INC. SPS 120-15

COMPUTER HARDWARE INC.



D3 VOLTS	R12
5.9 - 6.09	330Ω
6.1 + 6.29	300Ω
6.3 - 6.49	270Ω

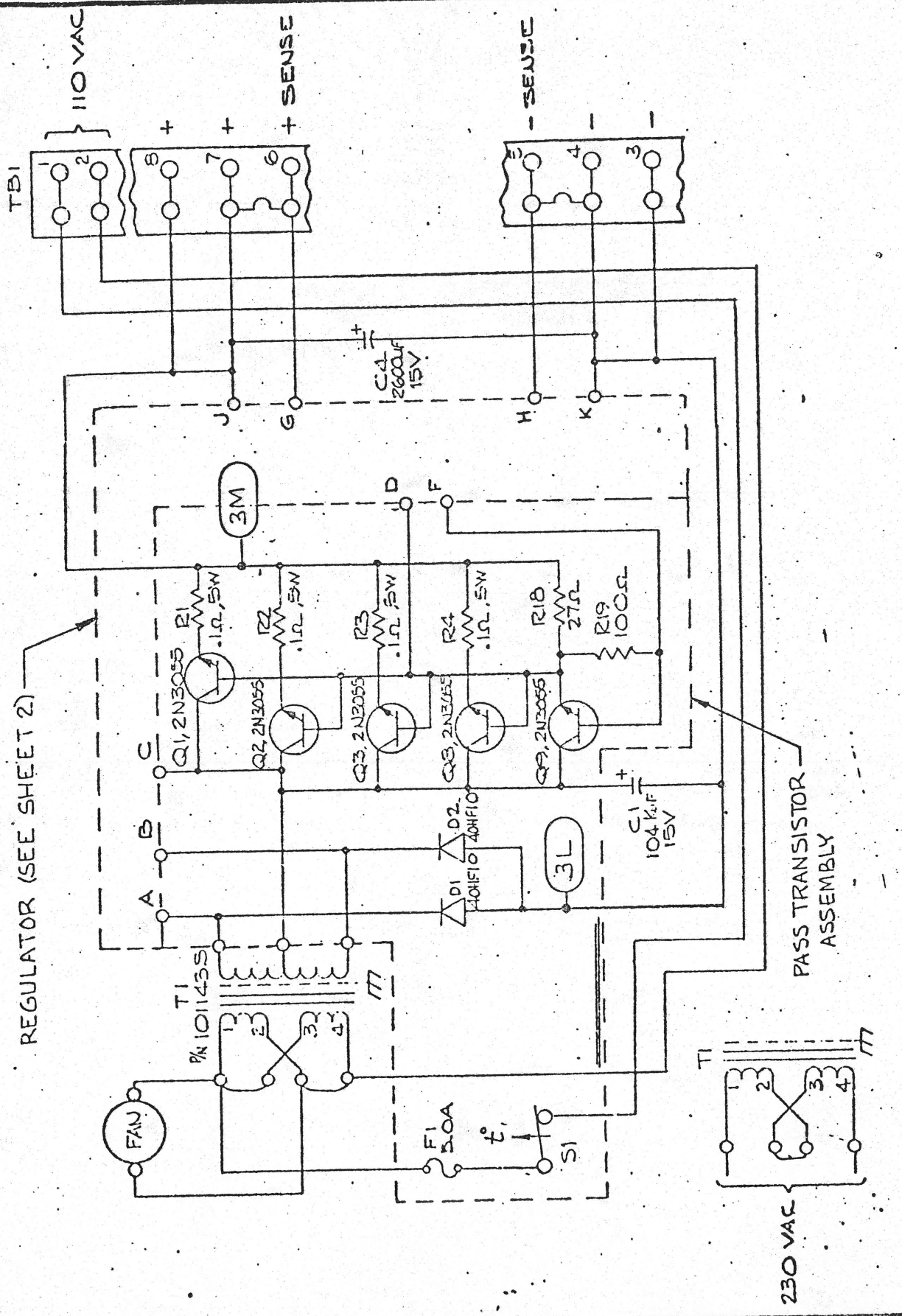
NOTE:
1. ALL RESISTORS ARE 1/2 W UNLESS NOTED.

TYPE-SIZE	DWG. NO.	REV. LET
SA	2163	NC
	SHEET _1_ OF _1_	

TITLE

POWER SUPPLY, 4.3-5.7VDC, 250W
STANDARD POWER INC. SPS 250-5

COMPUTER HARDWARE INC.



NOTE:

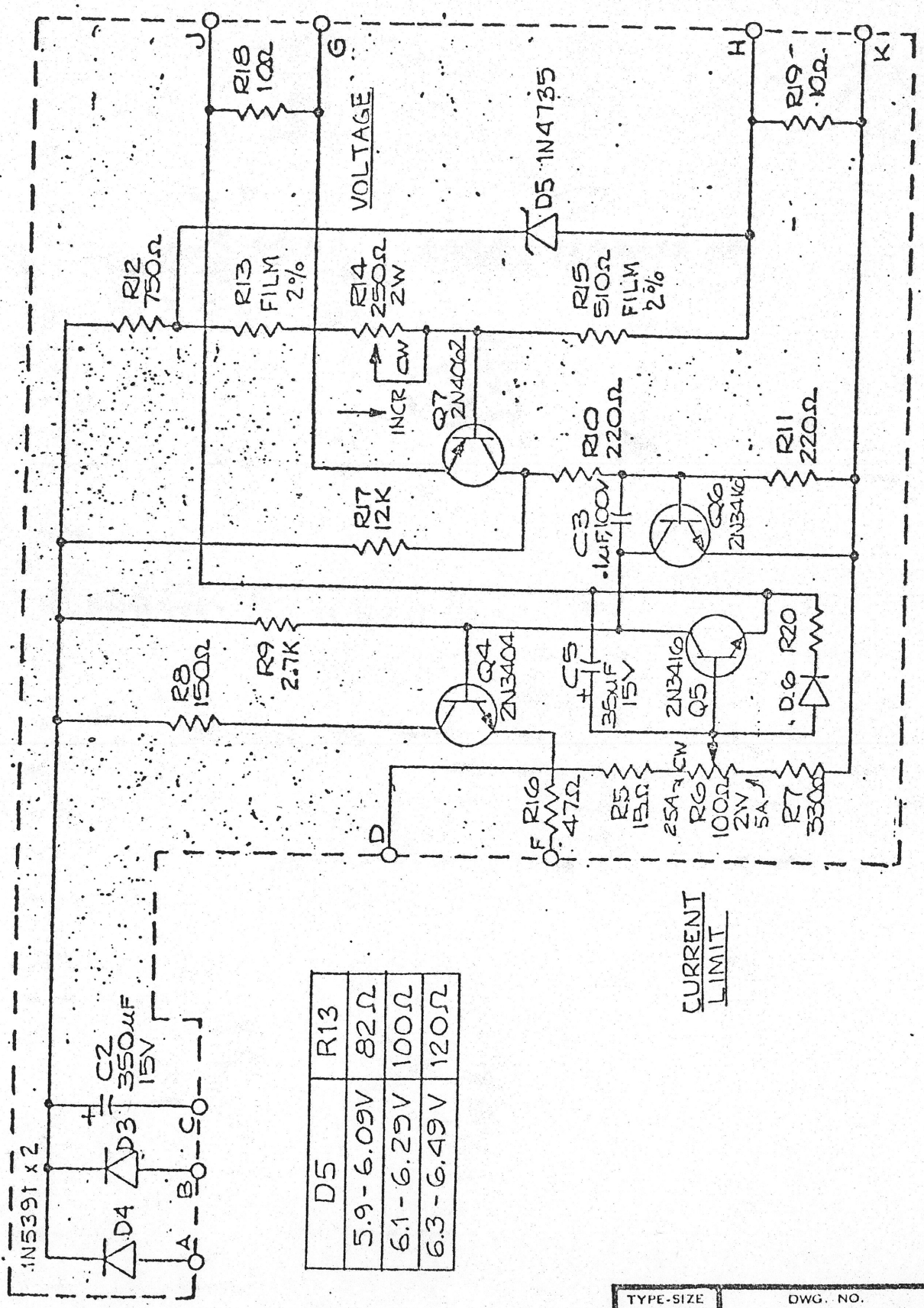
1. ALL RESISTORS .5W UNLESS NOTED.
2. SEPARATE REFERENCE DESIGNATIONS USED FOR OVP CIRCUIT (SHEET 3).

TYPE-SIZE	DWG. NO.	REV. LET.
SA	2340	NC
	SHEET 1 OF 3	

TITLE

POWER SUPPLY, 4.3-5.7VDC, 250W
STANDARD POWER SPS 250-5

COMPUTER HARDWARE INC.



D5	R13
5.9 - 6.09V	82Ω
6.1 - 6.29V	100Ω
6.3 - 6.49V	120Ω

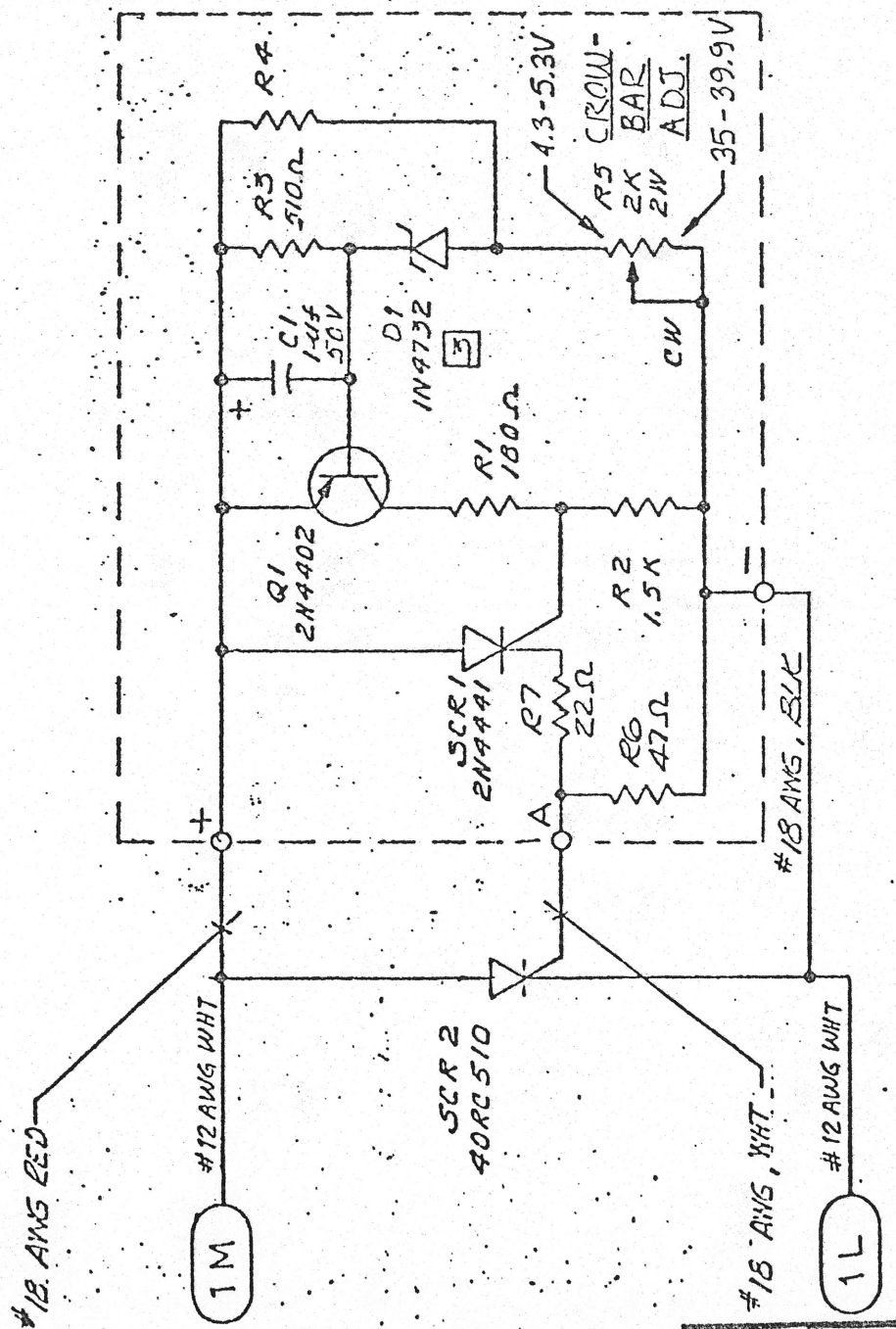
TYPE-SIZE	DWG. NO.	REV. LET.
SA	2340	
	SHEET 2 OF 3	

TITLE

POWER SUPPLY, 4.3-5.7VDC, 250W
STANDARD POWER INC. SPS 250-12

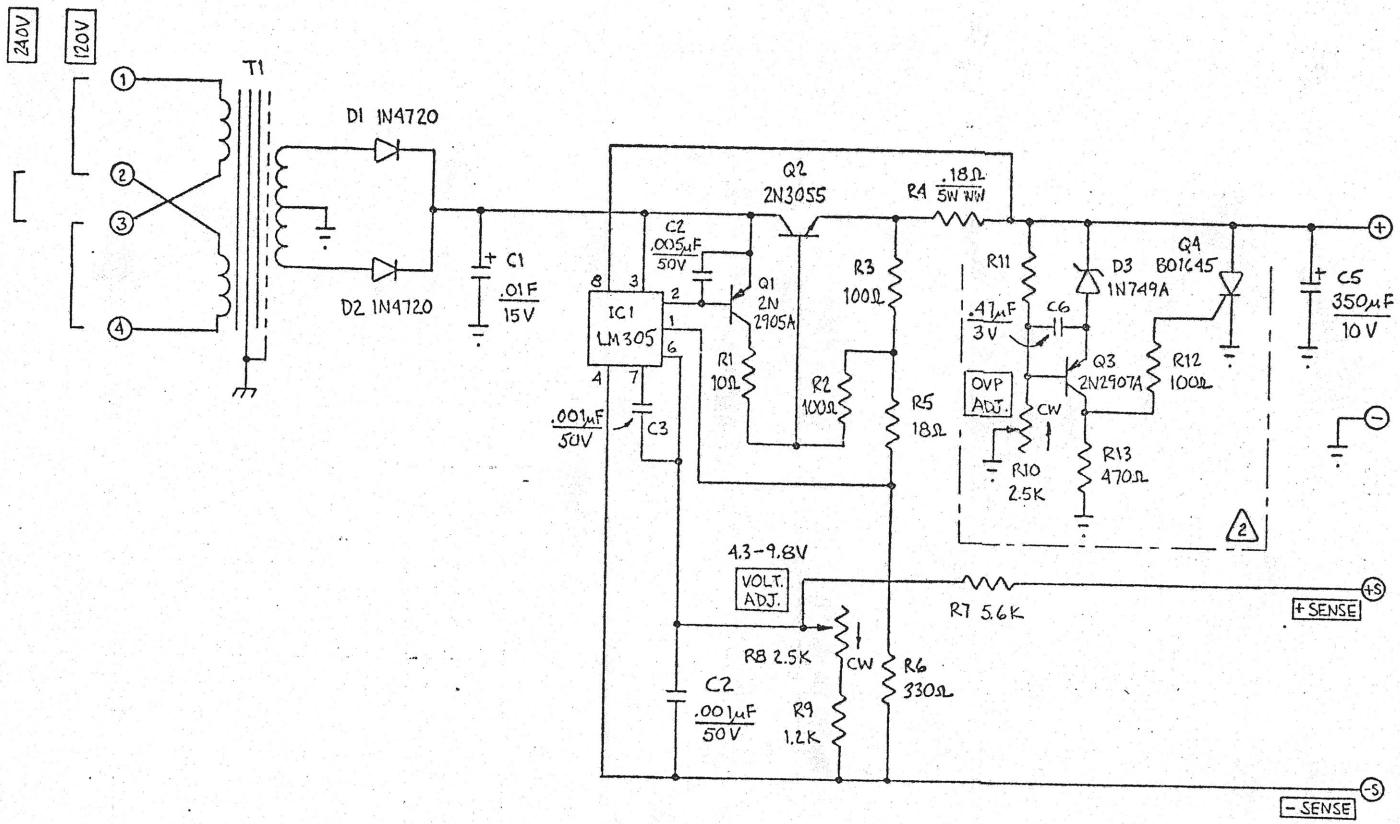
COMPUTER HARDWARE INC.

D1	R4
4.3V	270Ω
4.4-4.59V	330Ω
4.6-4.7V	360Ω



OVP-3 OVERVOLTAGE PROTECTION CIRCUIT

TYPE-SIZE	DWG. NO.	REV. LET.
SA	2340	
	SHEET 3 OF 3	



NOTES:

1. USED WITH PN XE-15-5 OVP, XENTEK INC.
2. OVERVOLTAGE PROTECTION CIRCUIT MAY BE ON SEPARATE PC BOARD ON SOME UNITS.
3. SETUP: TURN R10 FULL CCW. SET R8 TO OVP CIRCUIT LIMIT VOLTAGE (SEE NEXT HIGHER DRAWING FOR VALUE). TURN R10 CW UNTIL OVP CIRCUIT OPERATES (OUTPUT FALLS TO ≈1V.). REMOVE POWER. TURN R8 FULL CCW. APPLY POWER AND SET R8 TO OUTPUT VOLTAGE (SEE NEXT HIGHER DIAGRAM FOR VALUE). THIS PROCEDURE FOR REFERENCE ONLY; IT IS TO BE PERFORMED IN ACCORDANCE WITH THE NEXT HIGHER DRAWING.

CAUTION

DO NOT USE PART AS A REPLACEMENT. USE NEXT HIGHER ASSEMBLY WHICH WILL HAVE LEADS, PART MARKINGS AND SEALED ADJUSTMENTS. AN INCORRECTLY ADJUSTED SUPPLY WILL CAUSE DAMAGE TO EQUIPMENT.

QTY. REQD.	PART OR FILE NUMBER	NOMENCLATURE	MFG. PART NO. OR MATERIAL	MFG. NAME OR SPECIFICATION	ITEM NO.
		LIST OF MATERIALS			

FILE NUMBER

LETTER	DIN	CHK	DATE
CHANGE RECORD NO.			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DIMENSION TOLERANCES
ANGULAR DIMENSION ±1°
DECIMAL 2 PLACE ± .020
DECIMAL 3 PLACE ± .010
BREAK SHARP EDGES MAX. INSIDE CORNERS MAX
ALL MACHINE SURFACES 125
CHAMFER ALL THREADS 45° x FULL THREAD (UNLESS)
DO NOT SCALE THIS PRINT

TITLE: +5 VDC POWER SUPPLY W/ OVP

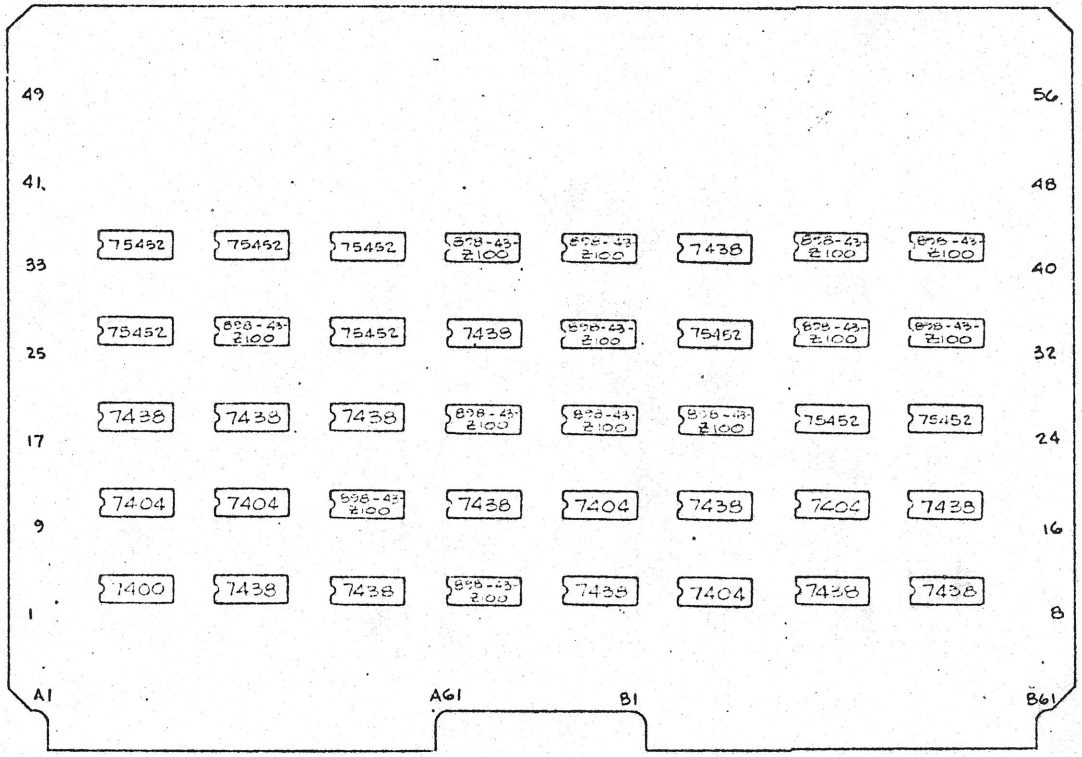
COMPUTER HARDWARE INC.

DRAWN	WHITEHEAD 6/15/73	CHECKED	MOYER 6/20/73
DESIGN	XENTEK INC.	TYPE-SIZE	SC
SCALE	NONE	DWG NO	1385
		SHEET	1 OF 1
		REV LET	NC

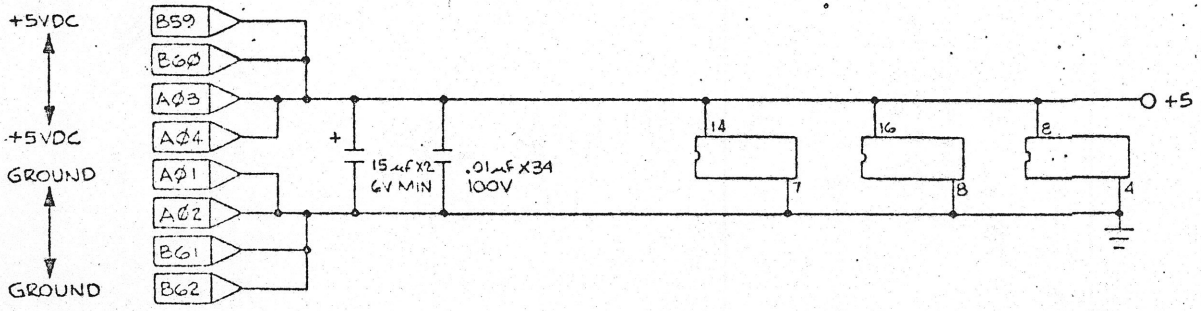
1385 SC

I/O CAGE

NOTES:
1. DELETED



ASSEMBLY REVISION DATA (REF)		
REV LETTER	DESCRIPTION	EFFECTIVITY
D	REACTIVATE DOUBLE SIDED PC BD ASSY	PROVIDE CYCLE-STEAL CYCLES CONCURRENT WITH SHIFT OPERATIONS



CONFIGURATION TABLE		
SC-2047	DC-2049	MC-2049
REV NC	REV NC	REV NC
A	NC	A
B	NC	B
C	NC	C
D	NC	D
D	NC	E

LAST USED TABLE	
CODE	REF. DES.
	IC 40

FILE NUMBER

		PART OR FILE NUMBER	NOMENCLATURE	MFG PART NO OR MATERIAL	MFG NAME OR SPECIFICATION	ITEM NO
QTY	REQD	LIST OF MATERIALS				

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DIMENSION TOLERANCES
ANGULAR DIMENSION ± 1°
DECIMAL 2 PLACE ± .020
DECIMAL 3 PLACE ± .010
BREAK SHARP EDGES MAX
INSIDE CORNERS MAX
ALL MACHINE SURFACES

LETTER	DRN	CHK	DATE

CHANGE RECORD NO

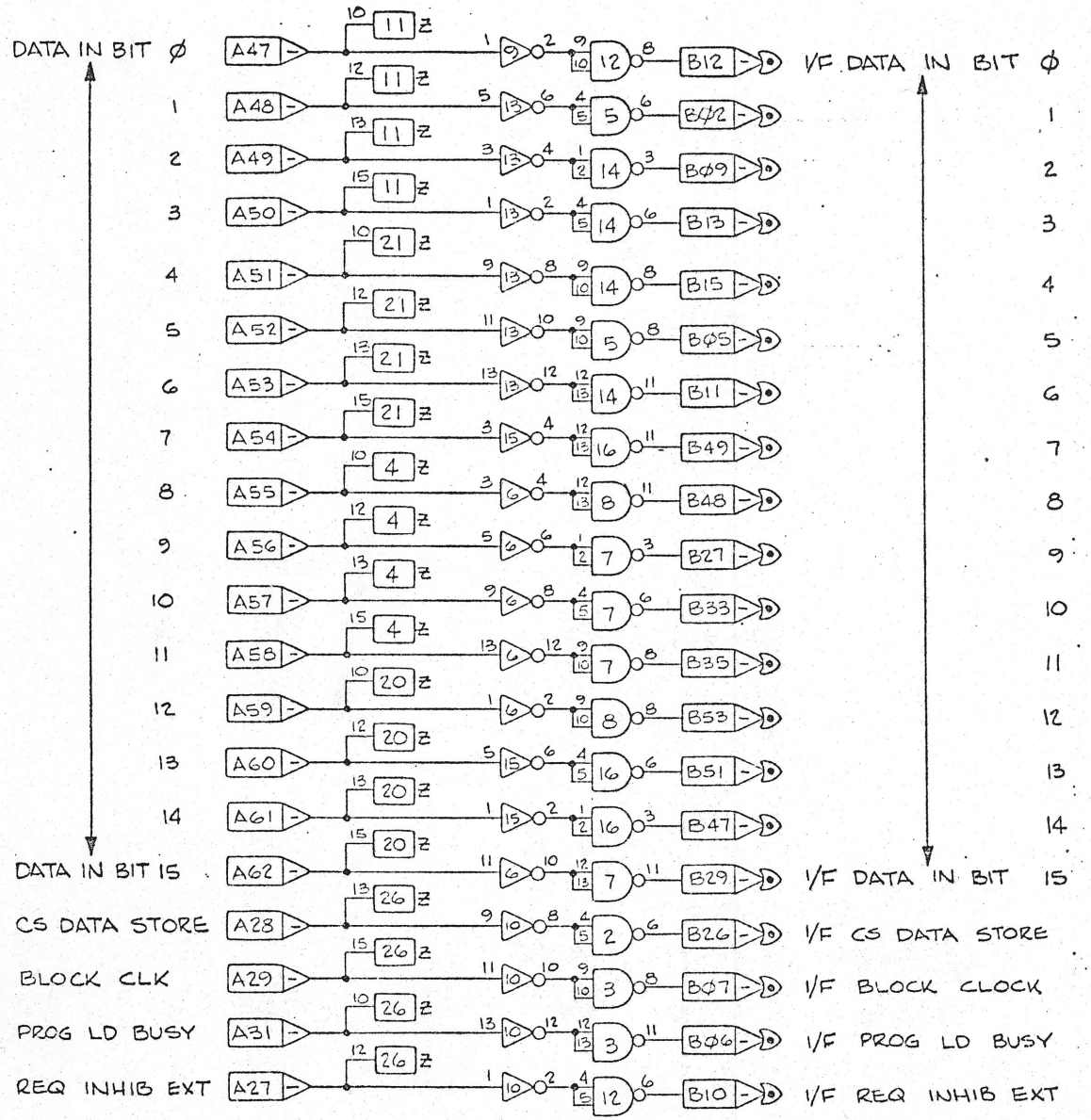
TITLE
COMMON ELECTRONICS W/I.F. TERMINATORS

COMPUTER HARDWARE INC.

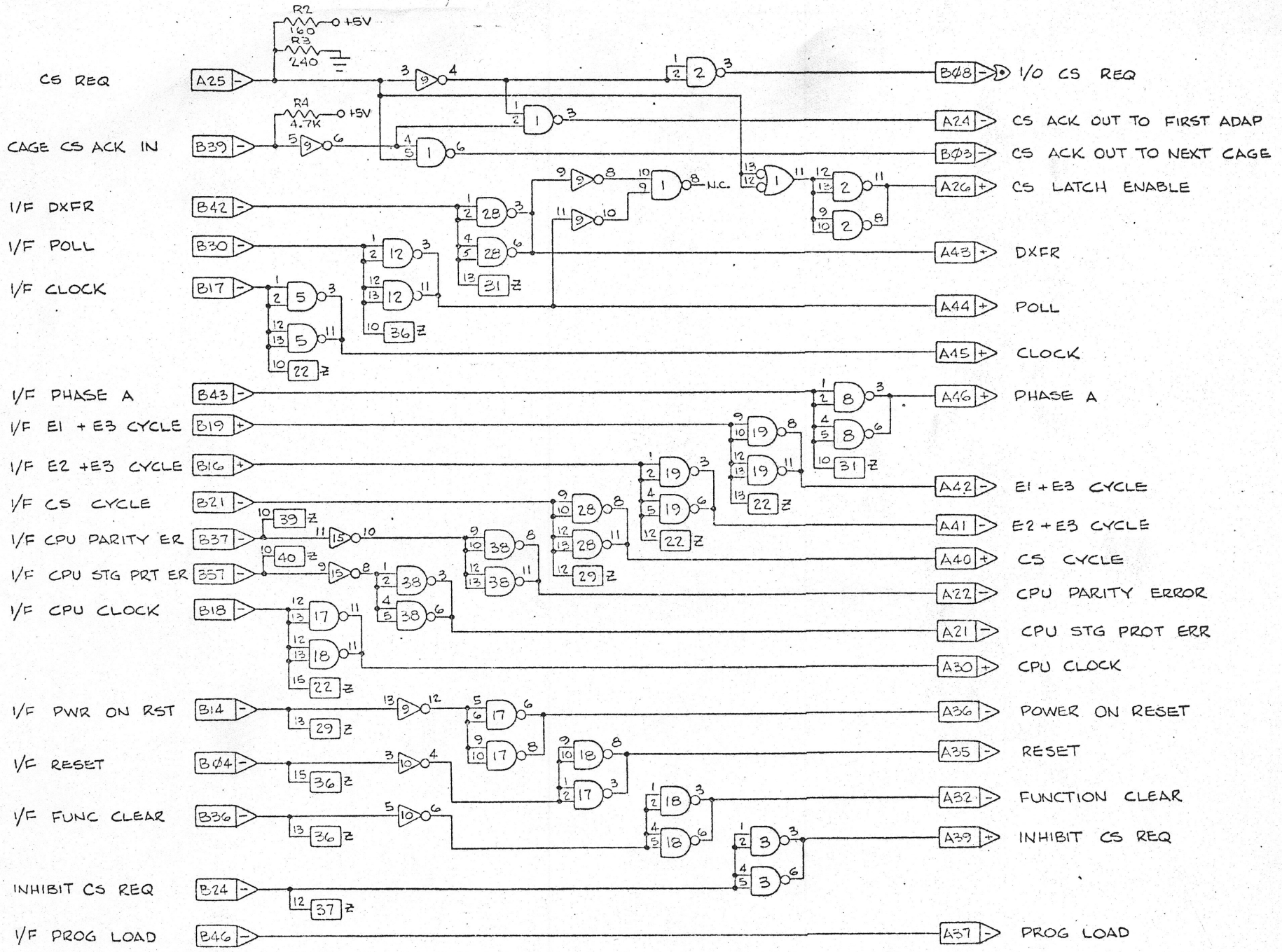
DRAWN | CHECKED
DESIGN
APPROVED
SIZE SC | DWG NO 2047 | REV LET D
SHEET 1 OF 2

DO NOT SCALE THIS PRINT

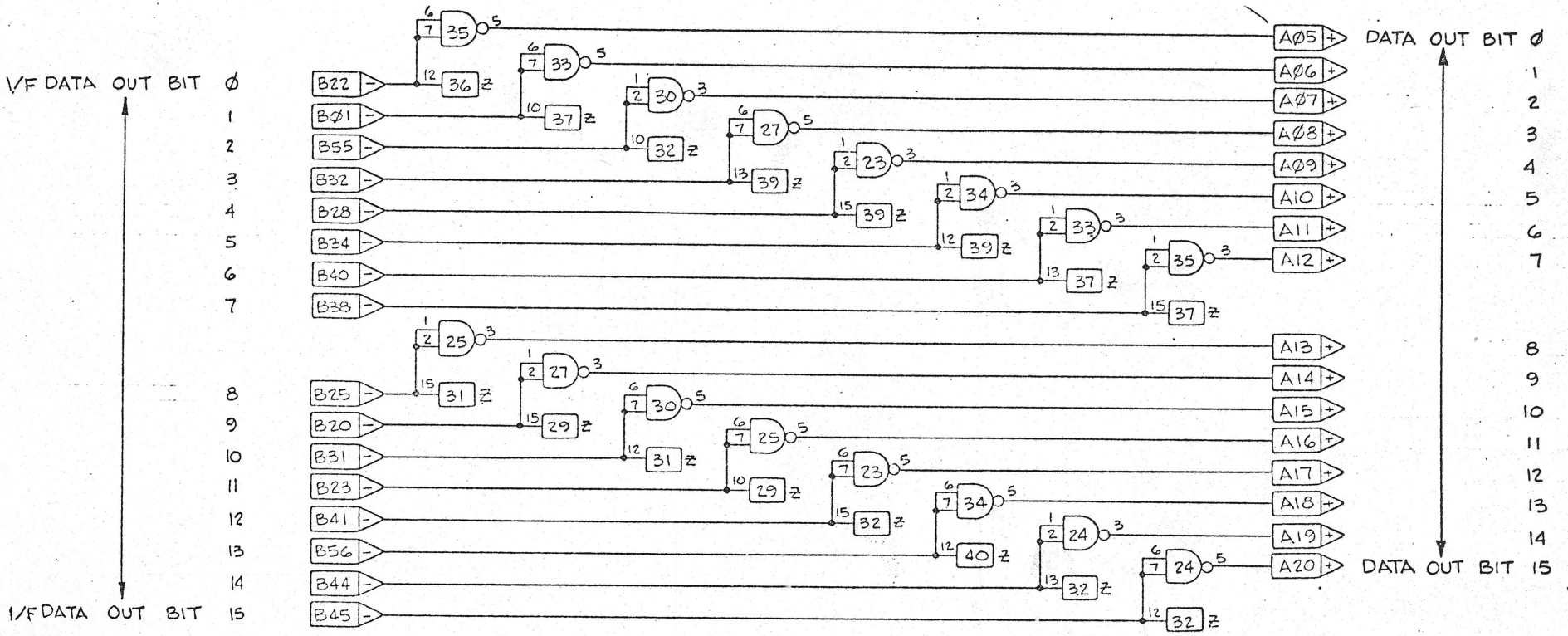
L 2047 INC



COMPUTER HARDWARE INC			
TYPE SIZE SC	DWG NO 2047 SHEET 2 OF 4	REV LET D1	



COMPUTER HARDWARE INC		
SIZE SC	DWG NO 2047 SHEET 3 OF 4	REV D1



B58 POWER LOSS INHIB

COMPUTER HARDWARE INC

TYPE-SIZE	DWG NO	REV LET
SC	2047 SHEET 4 OF 4	D1

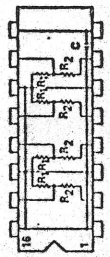
DATA OUT BIT 12 — 17
13 — 18
14 — 19
DATA OUT BIT 15 — 20
CPU CLOCK — 30
FUNC CLEAR — 32
RESET — 35
POWER ON RESET — 36
DXFR — 43
POLL — 44
CLOCK — 45
PHASE A — 46
INHIB CS REQ — 39
CS CYCLE — 40
E2 + E3 CYCLE — 41
E1 + E2 CYCLE — 42

DATA OUT BIT Ø — 5
1 — 6
2 — 7
3 — 8
4 — 9
5 — 10
6 — 11
7 — 12
8 — 13
9 — 14
10 — 15
DATA OUT BIT 11 — 16

CPU STG PROT — 21
CPU PARITY ER — 22
CS LATCH ENAB — 26

+5 Vdc — A3, A4
C1 .01 μf 100 V
GND — A1, A2

Z1 Z2 Z3 Z4 Z5 Z6 Z7 Z8



INTERNAL CIRCUIT
TYP. 8 PLACES

POSITION	PART
1 THRU 8	898-43-Z100

CONFIGURATION TABLE								
SC-2009	NC	NC	A					
PC-1913	NC	A	A					
AC-2032	NC	A	B					

QTY REQD	PART OR FILE NUMBER	NOMENCLATURE	MFG. PART NO. OR MATERIAL	MFG. NAME OR SPECIFICATION	ITEM NO.
LIST OF MATERIALS					

FILE NUMBER

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LETTER	DRN	CHK	DATE
A	KAC	A.J.	7/11/75
CHANGE RECORD NO			2009

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DIMENSION TOLERANCES
ANGULAR DIMENSION ± 1/2°
DECIMAL 2 PLACE ± .020
DECIMAL 3 PLACE ± .010
BREAK SHARP EDGES MAX
INSIDE CORNERS MAX
ALL MACHINE SURFACES √
CHAMFER ALL THREADS 45° X 1 FULL THREAD (INT & EXT.)
DO NOT SCALE THIS PRINT

TITLE: TERMINATOR, I/O MOTHER BOARD

COMPUTER HARDWARE INC.

DRAWN	DON	04-25-74	CHECKED
DESIGN	TCW		
SCALE	NONE		

TYPE-SIZE: SC
DWG NO: 2009
SHEET 1 OF 1
REV LET: A

8-7-74

SC 2009